WHITE PAPER

Cypress' CapSense Successive Approximation Algorithm

By Robert Jania, Cypress Semiconductor Global Marketing Manager (RJO)

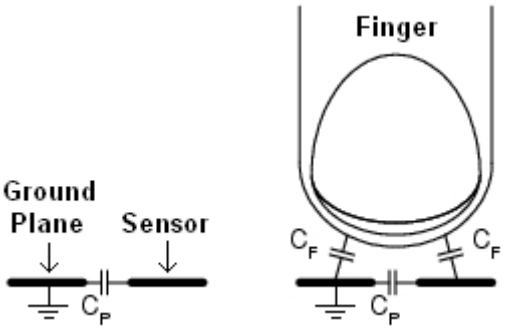
Executive Summary

Successive Approximation algorithm (CSA) is Cypress's new capacitive sensing algorithm for the CY8C20x34 PSoC® device family. CSA enables the implementation of an array of capacitive sensors through switched capacitor circuitry, an analog multiplexer and digital counting functions. The hardware configuration works in conjunction with high-level software routines from the CSA User Module found in PSoC Designer™ to compensate for environmental and physical sensor variations.

What is Capacitive Sensing?

A capacitive sensor is a pair of adjacent electrodes (Figure 1). When a conductive object is placed in proximity of the two electrodes, the capacitance is changed. The base capacitance is often referred to as the parasitic capacitance (C_P). The physical sensor itself is typically a copper trace constructed on a PCB. Sensors can be any conductive material. For example, one could use indium tin oxide (ITO) and print the pattern on a transparent substrate.

Figure 1. Capacitive Sensor

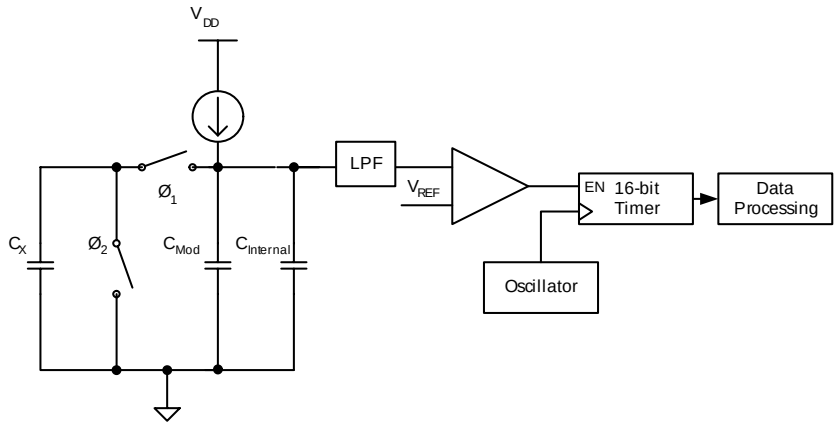


What is Successive Approximation?

The successive approximation method, developed by Cypress, uses the PSoC's switched capacitor circuitry to convert capacitance into a voltage. The voltage is then measured using a counter and a single-slope ADC. The capacitance measurement is achieved by converting the capacitance to its equivalent resistance, using the equivalent resistance to set and maintain voltage on a capacitor, then measuring the sampled voltage using an adjustable current source.

In addition to the sensor capacitor, CSA uses an internal capacitor ($C_{Internal}$) and an optional external modification capacitor (C_{Mod}). The block diagram for CSA appears in Figure 2.

Figure 2. CSA Block Diagram



The circuitry brings the sensor capacitor to a voltage relative to the capacitance of the sensor. The PSoC's internal main oscillator (IMO) clocks the switched capacitor.

To fully understand how CSA functions, it is useful to look at the actual waveforms of CSA. Figure 3 below shows the CSA waveform seen by probing C_{Mod} in a project with a single sensor and no finger present. Three regions can be seen in the CSA waveform. Table 1 describes the regions that can be seen in Figure 3. Each region is described in more detail in the following sections.

Figure 3. CSA Waveform Seen at C_{Mod} with no Finger Present

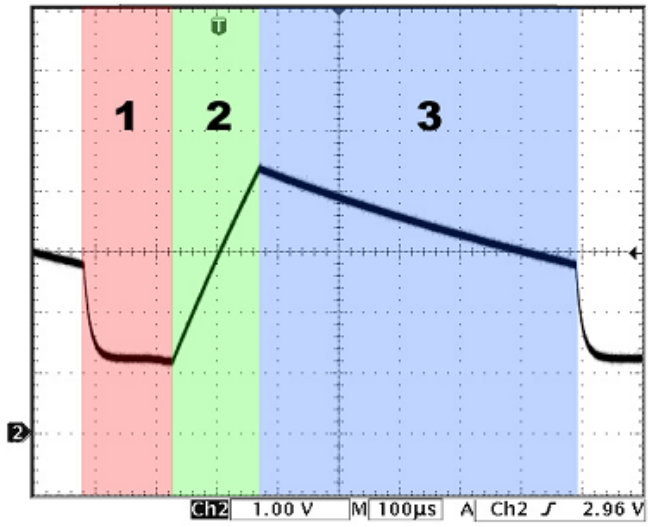


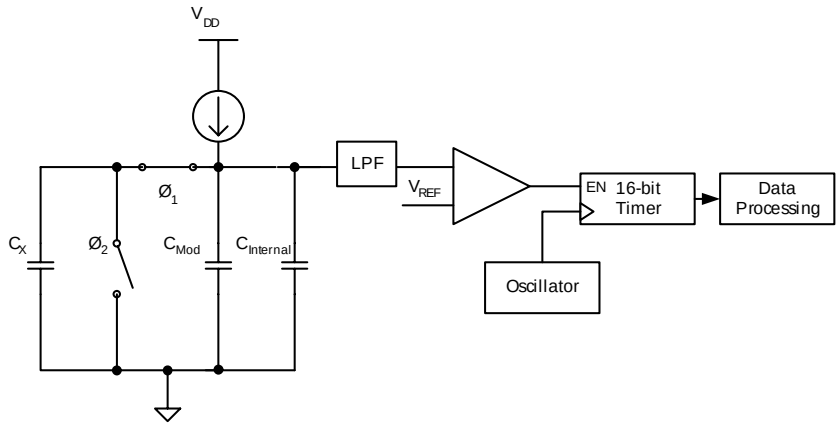
Table 1. CSA Waveform Regions

Region	Description
1	The sensor capacitor (CX) is connected on and off of the bus until voltage on the bus settles to V_{Start}.
2	The bus is charged by the iDAC until the voltage exceeds VREF and the comparator trips.
3	The sensor scan is complete and the iDAC is turned off. Voltage on the bus decreases as charge is dissipated by the low pass filter (LPF) until the next scan begins. The amount of time that this voltage decreases is strictly dependant upon the firmware between each scan and the CPU clock speed.

Region 1

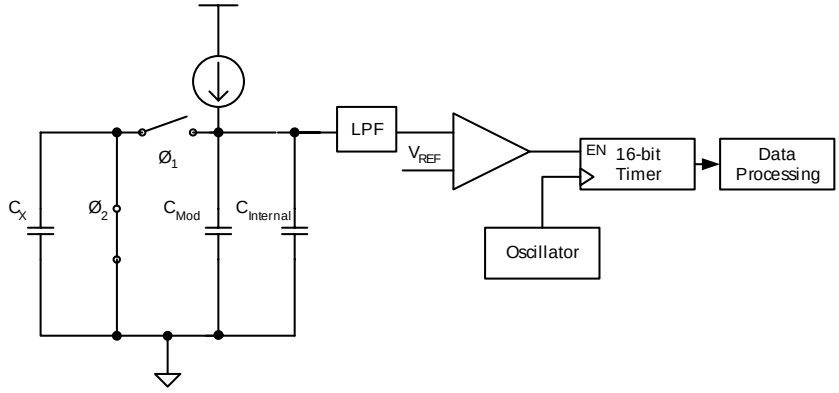
In Region 1 of the CSA waveform the sensor capacitor (C_X) is connected to the analog global bus, then grounded, in alternating phases. During phase 1 (ϕ_1), C_X is connected in the analog global bus in parallel with C_{Mod} and $C_{Internal}$. The block diagram of phase 1 is shown in Figure 4. $C_{Internal}$ and C_{Mod} share charge with C_X. Charge continues to flow onto C_{Mod} and $C_{Internal}$ from the iDAC current source.

Figure 4. CSA Block Diagram of Phase 1



Phase 2 (ϕ_2) disconnects C_X from the analog global bus and discharges C_X by connecting it to ground, leaving only C_{Mod} and $C_{Internal}$ connected. This is shown in Figure 5.

Figure 5. CSA Block Diagram of Phase 2



C_X is an effective resistance to ground through phases 1 and 2. An equivalent block diagram is shown in Figure 6. The equivalent resistance is given by:

$$R_{Equivalent} = \frac{1}{f_S C_X} \qquad \text{Equation 1}$$

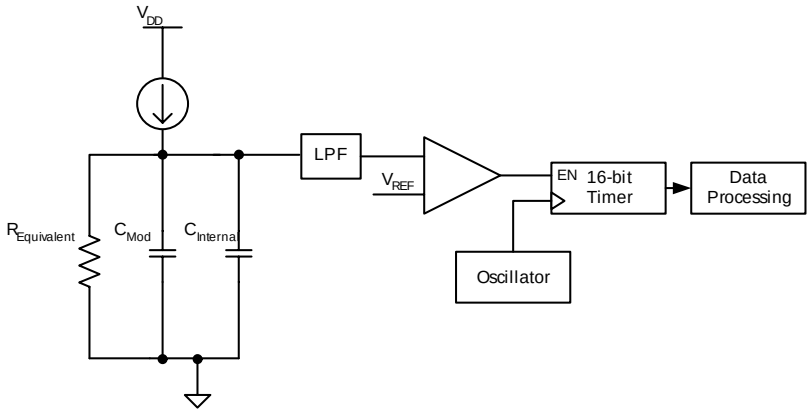
- f_S is the switching frequency of phases 1 and 2
- C_X is the sensor capacitance

The constant iDAC current flows through this resistance resulting in a voltage, V_{Start}. V_{Start} is given by:

$$V_{Start} = \frac{1}{f_S C_X} I_{DAC} \qquad \text{Equation 2}$$

- iDAC is the iDAC current

Figure 6. CSA Block Diagram with Equivalent Resistor



V_{Start} is set to a value below V_{REF} with the switched capacitor circuit running. This is accomplished by tuning the iDAC through successive approximation, which uses a binary search to determine the appropriate iDAC setting. Once the bus has been charged to V_{Start}, the iDAC current setting that was used is stored, and the process is repeated for each sensor in the project.

Region 2

After the voltage on C_{Mod} and $C_{Internal}$ settle to V_{Start}, the measurement sequence begins. A counter clocked by the IMO is enabled. As the counter runs, the iDAC charges C_{Mod} and $C_{Internal}$ until the voltage on the capacitors reaches V_{REF}. At V_{REF}, the comparator disables the counter. The number of IMO clock cycles (referred to as counts) recorded by the counter is used to determine if a finger is present on a sensor. Counts are taken after each measurement sequence and compared to the baseline count number, a stored value with no finger present on the sensor. If the difference between the recorded counts and the baseline counts exceeds the finger threshold value, sensor activation is detected.

The presence of a finger on the sensor increases the capacitance (C_X) of the sensor, which decreases the equivalent resistance ($R_{Equivalent}$) formed by the switching of ϕ_1 and ϕ_2. This is evident in Equation 1. The lower resistance results in a lower voltage across the capacitors (C_{Mod} and $C_{Internal}$), which we will call V_{Finger}. Thus, it will take longer for the iDAC to charge the voltage on the bus from V_{Finger} to V_{REF} than it does from V_{Start} to V_{REF}. This results in more counts (i.e. object present) on the sensor. A graphical representation of the charge time on the bus with a finger present versus not present is shown in Figure 7. The waveform in Figure 8 shows the CSA waveform with a finger present, and verifies the longer count time by the counter.

Figure 7. Voltage on Bus with Finger and No Finger Present on Cx

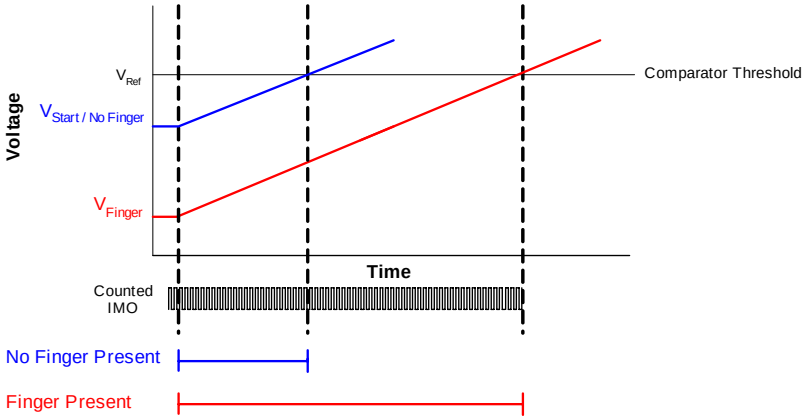
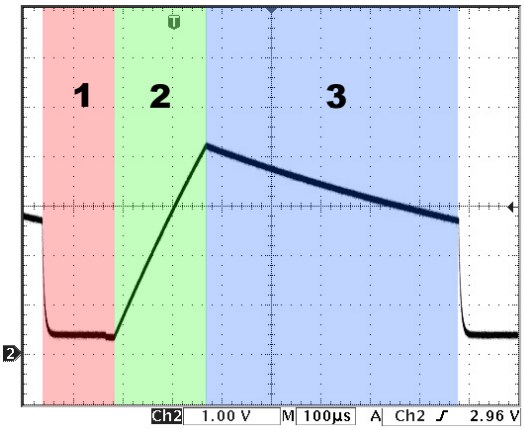


Figure 8. CSA Waveform Seen at Cmod with Finger Present



In Figure 8, the starting voltage in region 1 has dropped. This is due to the decrease in equivalent resistance, which itself is a result of the finger capacitance (C_F) added in parallel with the sensor capacitance (C_X). The charge time in region 2 is longer, resulting in more counts on the counter compared to no finger present on the sensor. An increase in charge time can be seen by comparing Figure 3 and Figure 8.

Region 3

In region 3 of the waveform the scan is complete and the iDAC is turned off. The voltage on the bus begins to drop due to charge dissipation by the Low Pass Filter (LPF) on the capacitor's input. The LPF is present to prevent the input of high frequency noise to the comparator. This voltage continues to decrease until the next scan sequence when the voltage is reset to V_{Start}. The amount of time that the voltage spends decreasing depends upon the firmware executed between each scan and the CPU clock frequency. A faster CPU clock frequency results in a smaller decrease in the voltage on the bus in region 3.

Noise Immunity

CSA offers high noise immunity, resulting in excellent sensitivity. Sensitivity is proportional to signal-to-noise ratio (SNR) levels. The switching of the sensor capacitor in CSA reduces the outside noise sources on the sensor capacitor that could inadvertently couple directly into the system. During phase 2, any noise introduced through the sensor capacitor is shorted directly to ground. In addition, the grounding of the sensor capacitor reduces the input impedance of the CSA system. The lower input impedance results in smaller voltages entering the CSA system as a result of any noise current.

The input of the comparator for CSA includes an internal LPF to reduce the effect of high frequency noise on sensor scans. External to the PSoC, an optional bus modification capacitor (C_{Mod}) further improves noise performance by acting as a bypass capacitor. The bypass capacitor prevents erroneous device interrupts by eliminating large voltage swings on the device inputs.

Summary

The PSoC Mixed-Signal Array is a configurable array of digital and analog resources, Flash memory, RAM, an 8-bit microcontroller and several other features. These features allow PSoC to implement innovative capacitive sensing techniques in its CapSense portfolio. PSoC's intuitive development environment can be used to configure and reconfigure the device to meet design specifications and specification changes. Successive Approximation exhibits exceptional sensitivity and noise immunity, low power consumption and a fast update rate, along with the flexible design process inherent to the PSoC.

For more information on PSoC, go to www.cypress.com. For more information on PSoC CapSense, visit www.cypress.com/capsense. For a more detailed explanation of the use of switched capacitors in the CSA algorithm, please see the CSA User Module Data Sheet inside PSoC Designer™ free at www.cypress.com/psocdesigner. For a comprehensive derivation of switched capacitor equations, see AN2041, "Understanding Switched Capacitor Analog Blocks" at www.cypress.com/design/AN2041, or reference Design With Operational Amplifiers and Analog Integrated Circuits, by Sergio Franco.

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709
Phone: 408-943-2600
Fax: 408-943-4730
http://www.cypress.com