One Hour Cycle Time from Die Attach through Final Tape and Reel for Semiconductor IC Manufacturing – Is it a Dream or a Reality?

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Biography
Bo Soon Chang started his technical career as a Semiconductor back-end process engineer at Fairchild Semiconductor, Korea in 1981. He was relocated to the Silicon Valley in 1986 to join Fairchild Semiconductor in Mt. View, CA. In 1987 he moved to National Semiconductor as an ASIC package engineer. He then joined Cypress Semiconductor in 1991, where he installed all the new packages for the Cypress Semiconductor, Philippines factory between 1995-1998. In 2000 he developed "The TRAILER", a fully integrated, in-line assembly-test-finish mechanism from die attach through tape and reel. Currently he is the Director of Technology Development Engineering for the new package and factory automation group in Cypress, CA.

Carl Gamboa joined the semiconductor industry in 1993 as a new package development engineer at Texas Instruments, Philippines. In 1998, he moved to Cypress Semiconductor, Philippines as a packaging engineer. While in Cypress, Philippines, he was involved in the development of "The TRAILER" for FBGA and leaded plastic packages. In 2001, he was relocated to Cypress, San Jose and is currently working with factory automation projects. He holds a BS in Electrical Engineering from Saint Louis University, Baguio City, Philippines.

Abstract:
The silicon wafers born at wafer FAB start a long journey to back-end manufacturing sites, mostly in Asia, to be assembled, tested and finished for the various customers around the world. This journey often takes several weeks.

Since cycle time is one of the most critical success factors in this journey, there have been a lot of efforts to reduce the manufacturing cycle time, either by factory automation, or by process simplification. However the cycle time in back-end operations has been limited to weeks in the typical scenario since the process flow in the semiconductor back-end industry is still a batch process and manual handling concept for each process step. No practical strip traceability and/or manufacturing process simplification has yet to emerge in significant volume manufacturing environments.

This paper will discuss the entitled cycle time for the back-end process flow in semiconductor factories and a case study reducing cycle time to less than one day. The most advanced integration flow in software as well as hardware has been achieved with various process simplification efforts such as "Get Out Of Human Eye Inspection" (GOOHEI), "Get Out Of Human Arm Movement" (GOOHAM) and "Get Out Of Human Intelligence Decision" (GOOHID).

Finally this paper will propose an aggressive challenge to one (1) hour cycle time for the entire process flow in real life. ***"Is it a dream or a reality ?"***

Introduction:
Cycle time is one of the most important indices in the operation performance of semiconductor manufacturing. Three main reasons why cycle time is important are as follows:

The first reason follows the saying "Cycle Time is Inventory and Inventory is Money, therefore

Cycle Time is Money". Batch processes and manual handling concepts maintain a high level of WIP inventory between each process step. Long cycle times tend to support a "Build-to-Forecast" planning philosophy. With reduced cycle times by factory automation and process simplification, "Build-to-Order" planning may be achieved. The advantages of the "Build-to-Order" are:

a. Factory can eliminate bulky and unnecessary inventory build-up by building only what the customer needs.
b. Since there is reduced WIP inventory, factory floor space is utilized more efficiently to build rather than store staged product.
c. Labor cost for inventory related maintenance activities is minimized or eliminated.
d. Paper work for material as well as data input in Management Information System (MIS) is significantly reduced.
e. A portion of Inventory built to forecast always has a tendency to age quickly to excess and/or obsolescence.

Secondly, the supply chain can be optimized since the factory only builds the volume needed by the customer. The material turnaround is fast enough, due to short manufacturing cycle time that the customer does not need to be concerned with maintaining their in-house incoming inventory. The factory can be more flexible with the customer's production demand in dynamic business situations. Furthermore, semiconductor manufacturing can be located adjacent to the customer's operation to supply true just in time supply from a lower value added state of inventory (die bank).

Thirdly, risk alleviation is faster with short cycle time resulting in:

a. Real time corrective action to any process faults.
b. Simplified tracking of affected materials in case of process faults.
c. Material rework or rejection can be maintained at minimum levels, with real time corrective action to process faults.

How did we determine our Eventual Cycle Time Goal?

Cypress' eventual cycle time goal is one hour from die attach to final tape and reel. This might be considered impossible, however, with advanced hardware and software integration supported by a high level of integratable process simplification, it may be **"a wish comes true".**

In a previous paper entitled ""The TRAILER": A Fully Integrated Assembly-Test-Finish Line for Matrix Array Molded BGA", Cypress detailed how factory automation was achieved with hardware and software integration. Hardware integration focuses on combining, grouping, all the equipment in the manufacturing line by conveyor or robotic motion as well as automated vision inspections. Software integration focuses on integrating the process steps and individual equipment cell controllers into a full lot tracking and lot discrimination manufacturing execution system. Using a 2 dimensional (2d) dot matrix coding on the leadframes and vision technology for strip tracking, the Manufacturing Execution System (MES) is capable of monitoring critical equipment process control parameters and in maintaining lot integrity within a seamless flow of continuous manufacturing. The system maps each die location on a frame for subsequent acceptance or rejection at the final pack stage, based on the memory map results of the multiple vision and testing operations in the integrated flow.

In this paper, discussions will focus on achieving eventual cycle time goal through combining simplified processes with previously developed and executed hardware and software integration.

Process simplification entails developing new inline processes wherein Cypress Process Development Methodology (PDM) plays a key role. PDM steps can be summarized as:

1. PDM-1: Understanding how the process works and creating innovative solutions for simplifying the process. Questions such as "Should we?", "Can we?", or "What would the impact be?" helps in deciding whether we need to explore the idea.

2. PDM-2: Formal Design of Experiments (DOE) to support new process simplification and defining the optimum working process window.
3. PDM-3: Qualifying the new process to insure that such change would not affect the quality and reliability performance of the package.
4. PDM-4: Integrating the new process with known processes to support factory automation.
5. PDM-5: Releasing the new process in volume production ramps.

It is also important to understand how the materials will be handled in each process to support factory automation with shorter cycle time. Material handling can either be lot-based handling, magazine-based handling or a strip-based handling concept (Figure 1).

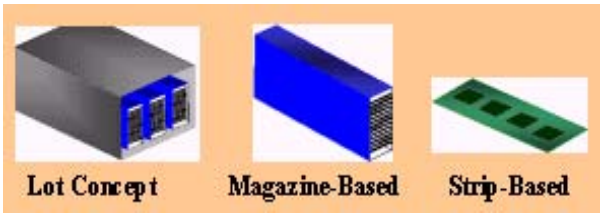


Figure 1: Material Handling Concepts

A theoretical cycle time comparison chart with these three cases is shown in Table 1.
A SSOP-56 Lead package is used as a model. The basic assumptions are:

a. One lot consists of 3.2K units.
b. One magazine consists of 40 strips.
c. One strip consists of 40 units.
d. No dry bake with MSL1 packages.
e. Handling, transport and queue time is not accounted for.

It may be noticed that strip-based handling has the shortest cycle time. The first unit comes out in about 8.3 hours and 3.2K units completed in almost 9 hours. Thus, strip-based handling proves to be a desirable approach for in-line process in view of cycle time.

In Figure 2, the FBGA and Leadframe process flows are shown. At each process step are corresponding in-line process developments (IPD). IPD's objective is to simplify the existing process by making it capable to integrate with various processes in order to support hardware and software integration with the least cycle time.

Process Step	Process Time (Hours)		
	Lot Based	Magazine Based	Strip Based
Die Attach (D/A)	0.80	0.40	0.010
D/A Cure	1.00	1.00	0.017
Wire Bond	1.76	0.88	0.154
Molding	0.46	0.23	0.006
Post Mold Cure	6.00	6.00	6.000
Solder Plate	2.00	2.00	2.000
Trim	0.46	0.23	0.006
Test	0.80	0.40	0.010
Lasermark	0.53	0.27	0.007
Form	0.53	0.27	0.007
Finish	0.80	0.40	0.010
1st Strip Out	--	--	8.227
1st Magazine Out	--	12.08	--
Lot (3.2K units) Complete	15.14	12.48	9.017

Table 1: Summary of Cycle Time per Handling Concept

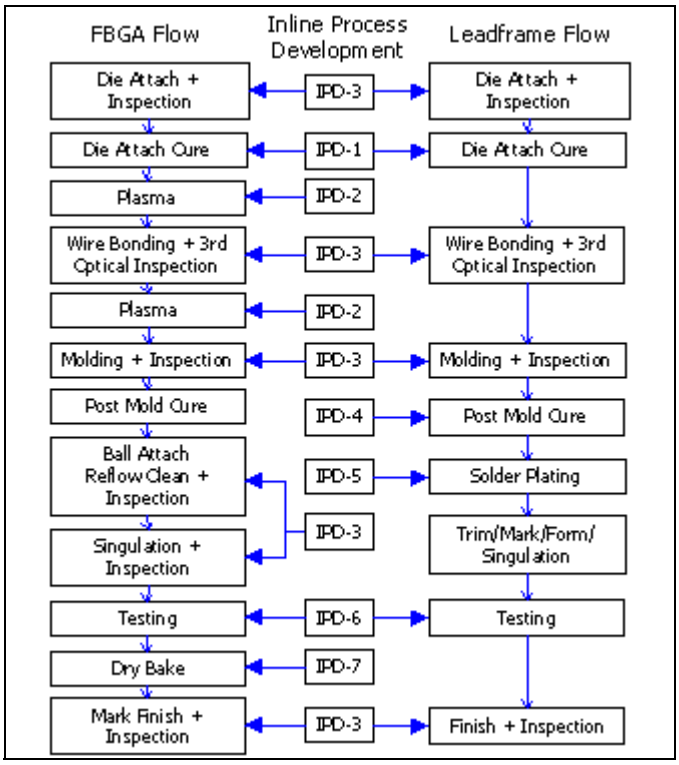


Figure 2: Inline Process Development Chart

Each IPD's critical success factors are summarized in Table 2.

	Description	Critical Success Factor
IPD-1	Inline Snap Cure	Snap cure epoxy selection and process optimization
IPD-2	Inline Plasma for FBGA	Process gas type selection and process optimization
IPD-3	Automatic vision inspection to support GOOHEI	Macro and micro correlation between auto visions and human eyes inspection
IPD-4	No post mold cure	Package reliability and product electrical impact
IPD-5	PPF concept for leadframe package	Pre-plated frame selection, process optimization and cost
IPD-6	Minimum test time for in-line test	Die purification and Low cost tester (LCT) development
IPD-7	No dry bake	MSL1 or moisture weight analysis

Table 2: IPD Summary Table

We will now discuss the journey to successful IPD execution.

IPD-1: In-line Snap Cure

Conventional batch oven cure of one hour was replaced by in-line snap cure of 120 seconds for FBGA, and 60 seconds for Leadframe packages. In-line snap cure development initially focused on material selection. Four snap cure epoxies from different suppliers were considered. The screening procedures are as follows:

a. Define optimum process set up for each snap cure epoxy with initial L8 Taguchi design of experiments (DOE).
b. Verify optimum process set up with confirmation runs.
c. Assemble different die sizes with working processes and materials.

Cure time and temperature are the Taguchi DOE factors. The quality observables are x-ray voids, resin bleed, cold die shear and hot die shear after cure. The screening shows higher percentage of voids after cure with larger die due to the area of trapped moisture between die and substrate or leadframe. The best candidate snap cure material showed less than a 5% void for a 80x80 mil^2 and 250x250 mil^2 die size and less than a 10% void for 400x400 mil^2 die size (Figure 3).

Two considerations in the selection of snap cure epoxy are its cure kinetics and rheology. The snap cure epoxy selected based on above screening procedure holds the following properties:

- Solvent-free (100% solids) for void free die attach. The adhesive contains no diluents, solvents or by-products that volatilize during curing.
- Very low moisture absorption with hydrophobic bismaleimide resin.
- Adhesive formulated with ultra-low temperature curing agents that permit the formation of void free die bonds.

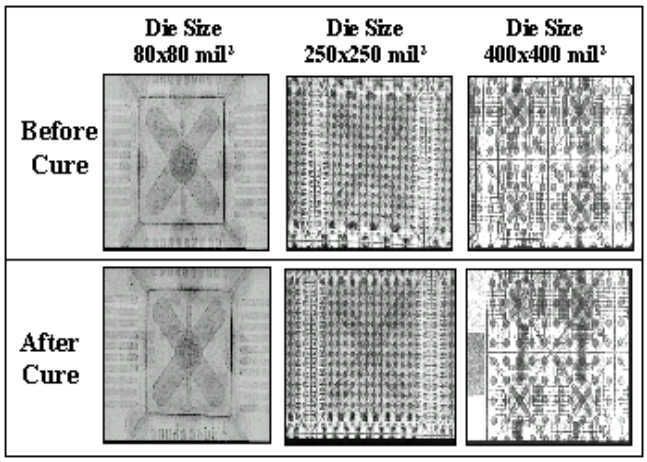


Figure 3: FBGA- Die Size vs Voids After Cure

The cure time as a function of weight loss and die shear was also experimented for leadframe packages in "The TRAILER". The data shows that at 60 seconds of cure, percent weight loss as well as die shear starts to normalize (Figure 4). Thus, a cure time of 60 seconds is safe for the snap cure process.

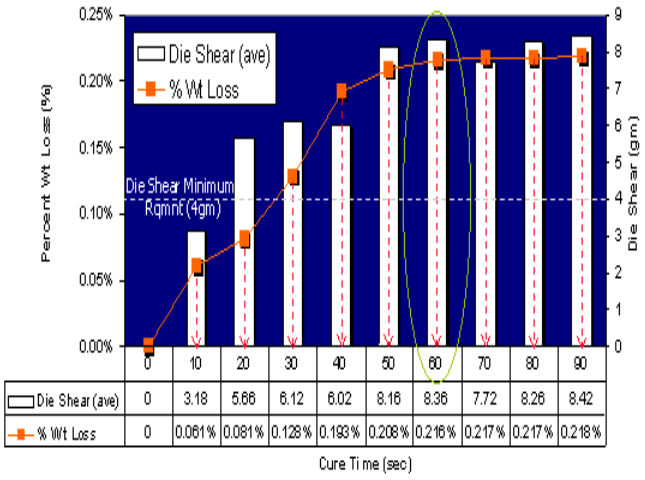


Figure 4: Weight Loss/Die Shear vs Cure Time Study

IPD-2: In-line Plasma for FBGA

Conventional magazine-based plasma cleaning was replaced by in-line strip plasma. Plasma cleaning in "The TRAILER" for FBGA is done for two reasons:

a. To clean conductive surfaces by removing organic contaminants (photo resist used during substrate etching, epoxy bleed-out) on lead fingers, solder pads or metallization.
b. To clean non-conductive surfaces, improving adhesion during molding due to increased surface energy of solder mask layer by roughening and "activating" the surface.

Typical gas types used in plasma cleaning are argon and oxygen or a combination of both. Argon plasma is used to physically remove contaminants from the surfaces. Oxygen plasma is used to create a chemical reaction to remove extremely thick carbon contaminants. An experiment was run on combining different percentages of argon (Ar) with Oxygen (O_2) and comparing surface treatment results with pure oxygen and pure argon. The results showed no significant change in surface treatment quality.

The decision to utilize 100% argon for plasma cleaning was based on the following:

- There is no significant benefit of using mixture of Ar/O_2 for "The TRAILER".
- Excessive oxygen may damage the bond fingers.

A 2-level, 3-factor full factorial design of experiments was conducted to establish optimum parameters for in-line strip plasma. The plasma parameters are power, pressure and time. The output response is a contact angle of water drop. A lesser contact angle of water drop is preferred, since it insinuates increased surface activation of the material. The contact angle of water drop before plasma typically ranges from 80 – 90 degrees.

In Figure 5, the DOE corner runs with its resulting contact angle of water drop are plotted. All DOE corner runs showed an average contact angle of water drop less than 20 degrees.

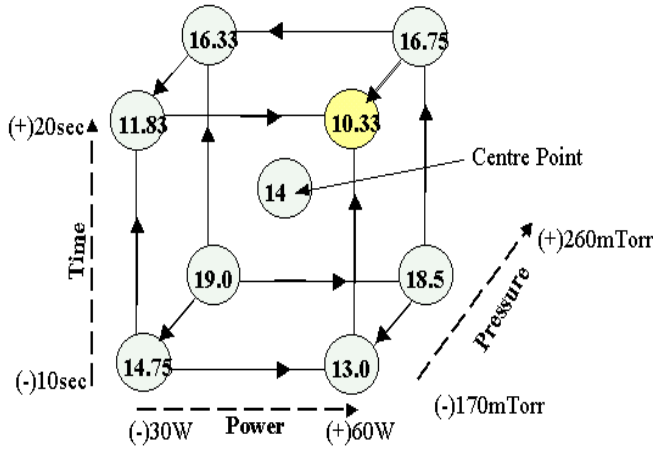


Figure 5:DOE Response Plot

IPD-3: Auto Vision Inspection to Support GOOHEI

The objective of "get out of human eye inspection" (GOOHEI) is to replace all human eye post process inspection in "The TRAILER" by 100% auto vision camera inspection at die attach, wire bond, mold, ball attach, saw, mark and tape and reel.

The critical success factors in the implementation of GOOHEI are micro-correlation and macro-correlation between human eye inspection and auto vision camera inspection.

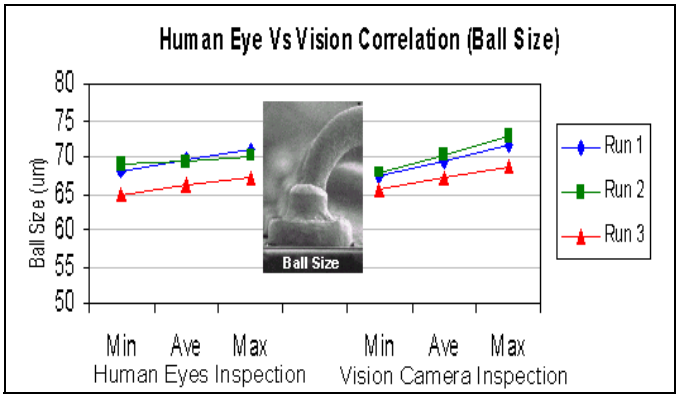


Figure 6: Vision vs Human Eye Micro-Correlation

Micro-correlation deals with correlating a known parameter or measurement as inspected by a vision camera and by human eyes, using calibrated and accurate offline measuring tools. An example is shown in Figure 6. In the wire bonding process, a study was conducted to correlate ball size measurement by vision camera and ball size measurement by a comparator. The

minimum, average and maximum readings for repeated runs were plotted. The results showed a negligible deviation of 3 microns between measurements by vision camera and human eyes by offline measuring tool.

The accuracy and reliability of GOOHEI micro-correlation depends largely on accurate and regular calibration of vision cameras. "The TRAILER" has its process controls primed to support this scheme.

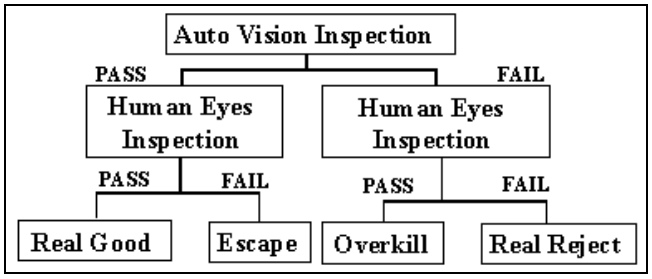


Figure 7: GOOHEI Inspection Output Category

Figure 7 represents GOOHEI macro-correlation. This study consists of evaluating and validating a considerable volume of units inspected by vision cameras. Overkill is a situation wherein vision cameras fail a unit, which is confirmed to be passing measurement criteria or parameter as inspected by human eyes. Escape is a situation wherein vision cameras accept a unit, which is confirmed to be failing measurement criteria or parameters as inspected by human eyes.

With extensive data collection and root cause-corrective action efforts, "The TRAILER" has successfully implemented GOOHEI by reducing overkill and escape to the level of current quality assurance (QA) sampling inspection in conventional line.

IPD-4: No Post Mold Cure for Leadframe Package

Post mold cure (PMC) is the second largest contributor to extended manufacturing cycle time besides dry bake. A big question raised by the author is "Why do we need to do post mold cure?" An engineer may answer, because of cross linking or Tg- glass transition, others may say because of possible delamination, if without PMC. These ideas sparked the author to initiate qualification, which eventually lead the way to eliminating PMC for specific Cypress products in "The TRAILER" for leadframe packages.

The considerations in eliminating the PMC process are package reliability, mechanical properties, and electrical performance. Table 3 shows the results of package reliability test and electrical performance verification by life burn-in test for two representative packages.

		With PMC Process	Without PMC Process
Package Type		TSSOP, SOIC	TSSOP, SOIC
Leadframe Finish		Ni/Pd/Au PPF	Ni/Pd/Au PPF
		Sn/Pb plating	Sn/Pb plating
Die Attach		Snap Cure	Snap Cure
Mold Compound	Cu	DCPD/BP	DCPD/BP
	PPF	OCN/BP	OCN/BP
MSL + Reflow		MSL1 235°C	MSL1 235°C
Package Reliability Response: C-SAM + (Electrical Test)			
Before MSL		Pass (0/15)	Pass (0/15)
After MSL		Pass (0/15)	Pass (0/15)
PCT		Pass (0/50)	Pass (0/50)
TCT		Pass (0/50)	Pass (0/50)
HAST		Pass (0/50)	Pass (0/50
Life Burn-In Test:			
EFR		Pass (0/250)	Pass (0/250)
LFR		Pass (0/120)	Pass (0/120)

Table 3: Reliability Data with No PMC

The results showed no significant influence of PMC with regards to the reliability of the package (ie. C-SAM, electrical test post stress) for Cypress products. A previous paper entitled "The Effect of Eliminating Post Mold Cure on Package Manufacturability, Reliability and Integrity for Memory Devices", dealt with the effect of PMC on package mechanical as well as electrical properties and concluded that there is no significant measurable performance degradation with the elimination of PMC.

"The TRAILER" for leadframe packages is running in production without PMC and ongoing quality monitors have revealed no quality and reliability issues related to PMC.

IPD-5: PPF Concept for Leadframe Package

The concept of pre-plated frame (PPF) was introduced to eliminate the offline batch solder plating process and enable the in-line assembly

and test process to not have any breaks in the continuous process. Industry available PPF technology options are solder PPF and palladium (Pd)-based PPF.

Solder PPF has a limited supply and poses manufacturing concerns. The process window for maximum temperature excursions is limited by the solder melting temperature on the frames. Pd-based PPFs provide a wide latitude in process temperature tolerance, requiring few, if any, changes to die attach, wire bond or mold processes.

Pd-based PPF options in the industry are four-layer nickel/palladium (Ni/Pd) and three-layer nickel/palladium/gold (Ni/Pd/Au). Four-layer Ni/Pd structure is a proven technology in the field. Three-layer Ni/Pd/Au is a relatively new Pd-based PPF.

We selected three-layer Ni/Pd/Au PPF because of the following compelling reasons:

- Three-layer Ni/Pd/Au PPF is less expensive than four-layer Ni/Pd PPF.
- Industry supports the three-layer Ni/Pd/Au PPF because of its enhanced wetting performance with both Tin/Lead (Sn/Pb) and Pb-Free solder alloys.

Three-layer Ni/Pd/Au PPF with Pd thickness of 0.8 *u*inch was qualified in "The TRAILER". We also started the process development for three-layer Ni/Pd/Au with Pd thickness of 0.2 *u*inch to align with industry's future direction to reduce cost.

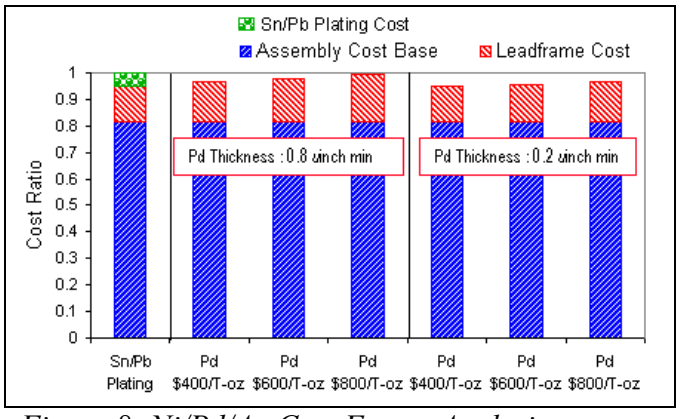


Figure 8: Ni/Pd/Au Cost Factor Analysis

Figure 8 shows a cost factor analysis with Ni/Pd/Au PPF and Sn/Pb solder plated leadframe. The cost of 0.8 *u*inch and 0.2 *u*inch Pd thickness at Pd-$400/Troy-oz, Pd-$600/Troy-oz and Pd-$800/Troy-oz are compared with Cu-Ag spot leadframe cost + inhouse Sn/Pb plating cost. Basically, the cost of Ni/Pd/Au PPF greatly depends on the Pd thickness wherein effective cost saving is realized with thinner Pd preplating.

Solderability with Pd-based PPF is another important consideration. Since Pd thickness is extremely thin as compared with Sn/Pb solder plating, it is very important that we minimize, if not eliminate, excessive lead contacts which may scratch the preplating layer and eventually expose underlaying metals.

Actual board mounting with Ni/Pd/Au PPF assembled package was carried out to evaluate its performance in an actual reflow environment. Sn/Pb solder plated and Ni/Pd/Au PPF assembled parts were mounted on same board and reflowed using standard reflow parameters. The lead cross sections revealed comparable solder joint formation between Sn/Pb solder plated and Ni/Pd/Au PPF assembled parts (Figure 9).

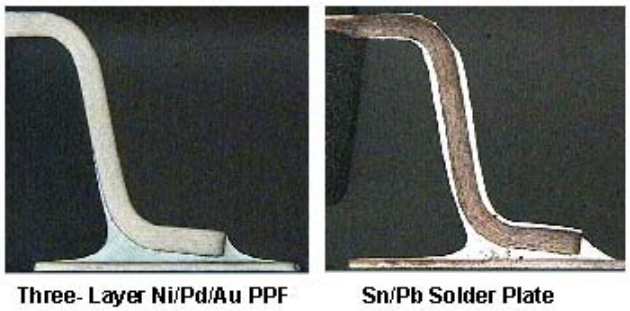


Figure 9: Solder Joint Formation

IPD-6: Minimum Test Time For In-line Test by CTAS / CTAC

Memory Products, as a general rule, require speed/power binning. At Wafer Fab, the wafers are subjected to a basic dc and parametric testing. Dynamic operating parameters of speed/power bins are not considered at the wafer test environment, due to the complexity of the hardware and engineering effort involved to simulate the packaged part response. . At Back-end Assembly and Test, the multi-bin wafers are

packaged and subjected to extensive electrical testing (includes speed/power binning) which usually results in long test cycle time. The Bin (speed/power) on demand is shipped to customers and the Bin with no demand is stored at Finish Goods (FG) inventory for future demand. Note that materials and capacity have been expended unnecessarily to build product without demand.

The objective of Class Test at Sort (CTAS) and Cheap Test at Class (CTAC) is to simplify the back-end electrical testing by electrically sorting the wafers at Wafer Fab to ensure the IC device meets all guaranteed operating parametrics and speed bins on the data sheet with sub 50ppm quality. This enables simple testing in the back-end test with Low Cost Testers (LCT) to screen out assembly damage and any burn-in drift fallout.

With CTAS flow, a wafer map file is created and then passed on to back-end Die Purification process. The Die Purification process consists of Backgrind, Wafer Mount, Wafer Saw and Die Sort operations (Figure 10). At the die sort process, the multi-bin die are sorted by bin onto individual storage mediums in the form of Gel Frames or Tape Film Frame. The bin with demand is shipped to back-end Assembly/Test and the bin with no demand goes to Die Bin Bank. The advantage of this flow is there is no need to invest manufacturing materials, time and capacity to build excess finished goods inventory for which there is no demand.

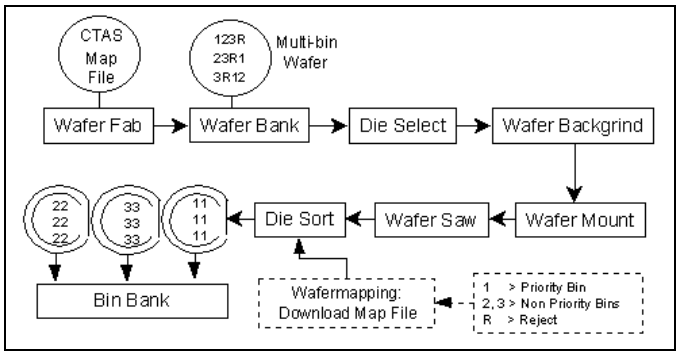


Figure 10: Die Purification Flow

Simple electrical testing (ie, open/shorts, minimum functional tests) at back-end test with CTAS flow and Die Purification process enables short cycle time making inline test viable with either multi-unit strip test in "The TRAILER" for leadframe packages or multi-unit singulated test for FBGA. In addition, CTAS flow enables the use of a standard configuration LCT (Low Cost Tester) with faster throughput at significantly lower cost to purchase and maintain. For example, LCTs typically cost 20 – 50k$ vs. the "Big Iron" testers at 500 – 3000k$. Existing "Big Iron" testers can be either sold, used for incremental capacity, or more likely transferred to the wafer sort area to increment the capacity of fully capable Class Test at Sort (CTAS) machines.

It becomes quickly apparent that CTAS not only provides significant capital avoidance but also provides yield improvement, cycle time reduction, and a not-so-subtle increase in engineering learning cycles as process related performance characteristic variations are seen immediately at the conclusion of the fab process.

Eventually, "The TRAILER" for FBGA requires further process and material developments to implement a higher throughput inline strip test flow via:

a. A Substrate designed to eliminate the "de-bussing" or singulation process.
b. A Device electrical performance warranty after singulation process.

IPD-7: No Dry Bake for FBGA in MSL3

The Dry Bake step is the longest process in the back-end assembly, typically requiring 24 hours. The purpose of dry bake is to remove the moisture that saturates within the package as a result of storage time, temperature and plastic moisture equilibrium solubility. Subjecting a package to reflow condition with certain level of moisture content may create popcorn effect resulting in package cracks and delaminations. In particular, this applies to surface mount packages wherein the board and the device are subjected to reflow temperatures.

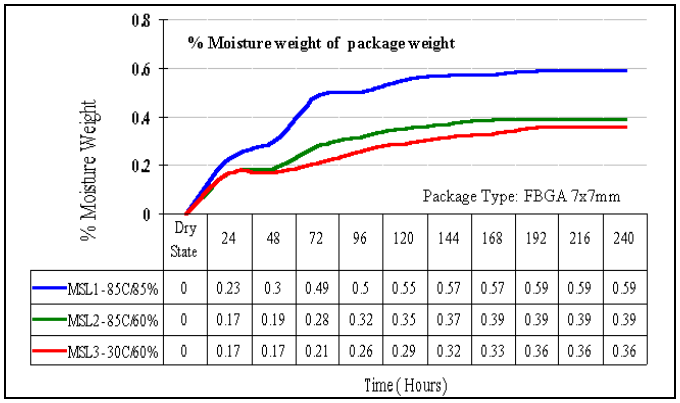
Packages that are qualified at Moisture Sensitivity Level 1 (MSL1) do not require dry bake and dry pack. Leadframe packages in "The TRAILER" are qualified at MSL1 with reflow temperature of 235^{o}C or 260 ^{o}C.

FBGA packages in "The TRAILER" are qualified at MSL3, however we managed to eliminate dry bake but with *dry pack* for small-outline FBGA of less than 100 square mm.

In reference to a previous paper entitled **"**The TRAILER": A Fully Integrated Assembly-Test-Finish Line for Matrix Array Molded BGA", the viability of eliminating Dry Bake by Post Mold Cure was discussed. Furthermore, the moisture weight within the FBGA package after the in-line flow was evaluated and results showed the moisture within the FBGA package is less than the current shipping moisture level in standard MSL3 dry-baked packages.

Further studies were done to insure that there would be no future reliability risks with shipping non-dry baked but dry packed FBGA packages. In order to eliminate dry bake with MSL3, the moisture level in the package should saturate at MSL3 preconditioning.

An experiment was run to determine moisture weight gain (absorption) at different MSL conditions (Figure 11). The weight gain analysis is very valuable in determining estimated floor life (the time from removal of a device from dry pack until it absorbs sufficient moisture to be at risk during reflow). At MSL3 soak condition of 192 hours at 30°C/60% RH, the %weight gain is approximately 0.36% of the package weight. This value will then be used as the baseline moisture weight saturation for non-dry baked MSL3 package.



	Dry State	24	48	72	96	120	144	168	192	216	240
MSL1-85C/85%	0	0.23	0.3	0.49	0.5	0.55	0.57	0.57	0.59	0.59	0.59
MSL2-85C/60%	0	0.17	0.19	0.28	0.32	0.35	0.37	0.39	0.39	0.39	0.39
MSL3-30C/60%	0	0.17	0.17	0.21	0.26	0.29	0.32	0.33	0.36	0.36	0.36

Figure11: Moisture Absorption Curve by MSL

The next step is obtaining moisture weight at different floor times representing the flow of material from factory to customer board mount. The eventual process flow for MSL3 FBGA non-dry bake package is shown in Figure 12.

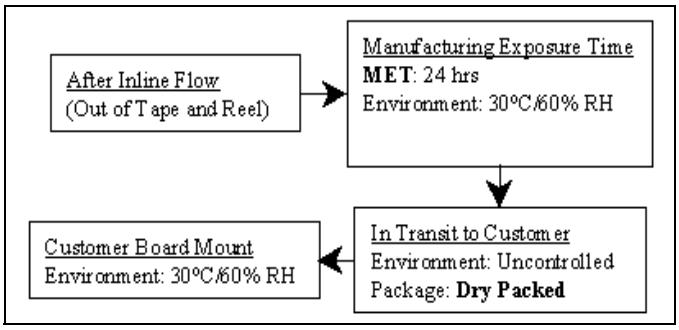


Figure 12: MSL3 FBGA Non-DryBake Flow

A representation of predicted moisture weight trend is shown in Figure 13. P1 represents the moisture weight after full in-line flow processing, P2 represents the total moisture weight of P1 and a Manufacturing Exposure Time (MET) of 24 hours. P3 represents total moisture weight of P1, P2 and one week floor life. One week floor life represents the allowable floor life of package after removal from dry pack bag at end customer site. P4 represents the total moisture weight of P1, P2, P3 and an additional one week of floor life as an extreme case.

Actual data gathered showed the moisture weight in the package becomes saturated after 192 hrs of 30°C/60% RH environment at less than 0.36% of the package weight. This implies that the level of moisture in the package is safe for reflow soldering even without a dry bake of 24 hours on the MSL3 FBGA package.

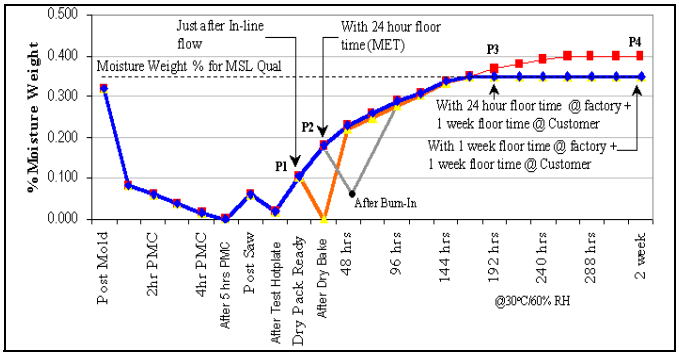


Figure 13: Representative Chart for Predicted Moisture Weight Trend

Where are we now?
The entitled cycle time with IPDs implemented in "The TRAILER" is shown in Figure 14.

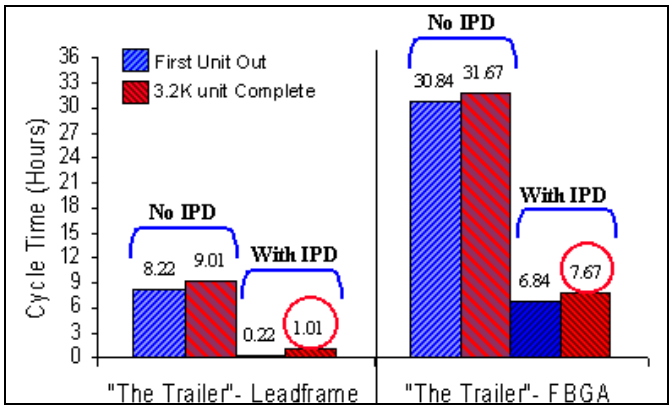


Figure 14: Cycle Time Summary Chart

Since the process simplification is not 100% matured as yet, actual cycle time is still much higher than the entitled cycle time with "The TRAILER" today. However, we are very confident that the entitled one (1) hour cycle time will be achievable with all the above IPDs implemented in "The TRAILER".

The one hour cycle time in "The TRAILER" for FBGA remains a challenge since the Post Mold Cure (PMC) process still exists in the FBGA process flow. Material and process development for package robustness at MSL1 will be the enabler to eliminate dry bake as well as PMC. The authors are looking forward to this as the final IPD step to realize the entitled cycle time of one hour in "The TRAILER" for FBGA packages too.

Conclusion:
A one hour cycle time from die attach through tape and reel for semiconductor IC manufacturing is no longer a visionary dream. Although not yet fully executed in today's Assembly and Test operation, the roadmap is now clear.

This paper has discussed and presented the process simplification steps to support hardware and software integration in view of what may be described as "The Factory Of The Future" in semiconductor IC manufacturing. The discussions herein are a means of sharing our current development studies and encouraging further industry development in methods and materials to facilitate the "one hour cycle time" in reality.

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