Golden Gloves ADC Championship Match – SAR vs. Sigma-Delta (ΣΔ)

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In one corner, the current Champion SAR ADC, in the opposing corner, a relative newcomer to the analog to digital conversion scene, the ΣΔ ADC.

This will be a 7-round fight to the finish, with judges awarding points in the following categories:

1. Conversion Accuracy
2. Speed of Conversion
3. Linearity of Strikes
4. Conversion Accuracy in the Low and High Side Corners
5. Differential Non Linearity
6. Integral Non Linearity
7. Quantization Error

Which will walk away with the title? Will it be the SAR ADC with its excess baggage (sampling and hold circuit), speed and indecision, or the light weight ΣΔ ADC with its integrating circuitry, and methodical and accurate thought process?

Round 1: Conversion Accuracy

Accuracy is a component of gain errors and non-linearity. Gain error will be discussed here and non-linearity errors will be touched upon in rounds 5 and 6.

There are two types of gain errors. Signal error due to scale is caused by variations in the reference and the gain channel between the input and the ADC, resulting in an error proportional to the signal level. Offset error is caused by a mismatch of input devices in input amplifiers and the op-amp used in the ADC's integrator/comparator.

In Fig 1, we can see ΣΔ's modulator (integrator, comparator, and 1-bit DAC) and digital filter. The ΣΔ ADC may contain a selectable gain amplifier on its front end. Changing the gain of the amplifier changes the size of the input sampling capacitors. Due to variations in the sampling capacitors, the gain may not be exact resulting in the requirement for ADC calibration. To correct for offset and gain errors, correction factors are derived from the zero, positive full-scale, and negative full-scale conversion results.

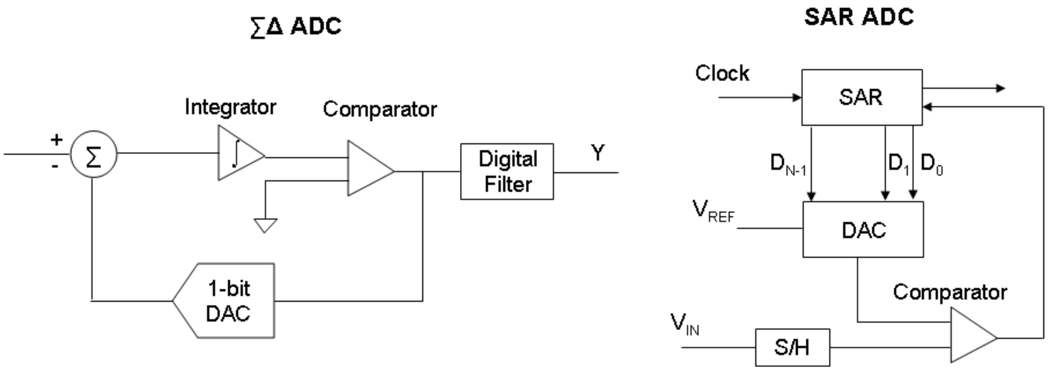

Figure 1: ΣΔ and SAR Topology

On the other hand, SAR ADC conversion accuracy is dependent upon the voltage reference, internal DAC, and comparator. The ADC's internal DAC and comparator must be made as accurate as the overall system – any inaccuracy results in linearity errors, which cannot be calibrated out.

Round 1 goes to the ΣΔ ADC due to it being inherently monotonic nature.

Round 2: Speed of Conversion

A ΣΔ converter requires 2^n samples to complete a conversion; therefore, conversion rate is a function of converter resolution and so higher resolution requires longer conversion time. Traditional ΣΔ converters commonly used in digital audio gear have bandwidths of around 22kHz. Recently, ΣΔ converters with bandwidths of 1MHz to 2MHz with 12 to 20 bits of resolution have been introduced to the market. These usually contain 4th (or higher) order sigma-delta modulators with multi-bit feedback DACs.

At the start of a SAR ADC conversion cycle, the DAC is set to half-scale and a comparison is made between the voltage to be measured and the DAC's output. With each step, the DAC is updated, the next bit selected, and a comparison made. The digital representation of the input voltage is found using a binary search ("successive approximation").

Round 2 goes to the SAR ADC due for its speed of the conversion algorithm.

Round 3: Linearity of Strikes

Both forms of non-linearity – differential non-linearity (DNL) and integral non-linearity (INL) – are functions of the topology and construction of the converter. DNL and INL errors cannot be calibrated out like gain and offset errors.

The accuracy of the ΣΔ ADC is dependent upon the settling of the op-amp in the integrator/comparator. If the modulator is switched too fast and the op-amp cannot keep up, nonlinearities will occur.

ΣΔ ADCs are inherently monotonic, no matter how many bits of resolution they provide. Performance is designed in and does not depend on exact component values or component matching.

In the SAR ADC linearity errors are related to the accuracy of the internal DAC and comparator. Linearity errors are a side effect of the SAR design.

Round 3 goes to the ΣΔ ADC.

Round 4: Conversion Accuracy in the Low and High Side Corners

A ΣΔ converter has increased nonlinearity at specific output codes. This is a function of the FIR filter used in the decimator. This nonlinearity occurs most prominently at the end-points of the scale. The end-point nonlinearity isn't a problem in continuous data streams such as digital audio; however, systems that require linear measurement rail-to-rail should not use ΣΔ converters.

The SAR ADC does not exhibit the large low- and high-side end-point inaccuracies of the ΣΔ converter. Its end-point accuracy is dependant upon the rail-to-rail tracking (voltage compliance) of the internal DAC and comparator.

Round 4 goes to the SAR ADC for its low- and high-side corner accuracy.

Round 5: Differential Nonlinearity

The differential nonlinearity error is the difference between an actual step and the ideal value of 1 LSB. Therefore, if the step width or height is exactly 1 LSB, then the differential nonlinearity error is zero. If the DNL exceeds 1 LSB, there is a possibility that the converter can become non-monotonic. This means that the magnitude of the output gets smaller for an increase in the magnitude of the input. In an ADC, there is also a possibility that there can be missing codes; i.e., one or more of the possible 2^n binary codes are never output.

ΣΔ ADCs are inherently monotonic, no matter how many bits of resolution they provide. Performance is designed in and does not depend on exact component values or component matching.

SAR ADCs are not inherently monotonic, and their performance depends on exact component values and component matching.

Round 5 goes to the ΣΔ ADC.

Round 6: Integral Non Linearity

Integral nonlinearity error is the deviation of the values on the actual transfer function from a straight line. This straight line can be either a best straight line as to minimize these deviations or it can be a line drawn between the end points of the transfer function once the gain and offset errors have been nullified. For an ADC, the deviations are measured at the transitions from one step to the next, and the name "integral nonlinearity" derives from the fact that the summation of the differential nonlinearities from the bottom up to a particular step determines the value of the integral nonlinearity at that step.

Round 6 goes to the ΣΔ ADC as its design does not depend on exact component matching or values. The SAR ADC, in contrast, requires a highly-accurate DAC and comparator.

Round 7: Quantization Error

Quantization error is due to the finite resolution of the ADC, and is an unavoidable imperfection in all types of ADC. It is a rounding error between the analog input voltage to the ADC and the output digitized value. The noise is nonlinear and signal-dependent.

ΣΔ converters require no anti-aliasing filters with steep roll-offs at the analog inputs due to the sampling rate being much higher than the effective bandwidth. Oversampling tends to average out any system noise at the analog inputs. Speed is traded for resolution in a ΣΔ converter.

The main advantages of SAR ADC's are low power consumption, high resolution, and accuracy. In a SAR ADC, increased resolution comes with the increased cost of more accurate internal component.

Even though the ΣΔ ADC took most of the rounds, the judges called it a draw. Both converters excel in specific applications. Selection of a ΣΔ or SAR ADC must be based on the signal to be quantized, conversion speed, conversion accuracy, and price. There is room for both. Nowhere is that clearer than in applications – from consumer and automotive to medical and industrial – where analog signals from the myriad sensors these devices contain must be detected, amplified, conditioned, and converted to enable their processing in the digital domain. SAR and ΣΔ, with their own pros and cons, have been adopted by designers based on the different specific application requirements. There is no question that both of them have separate stages on which to show off their "Kung Fu", so to speak.

Recognizing this, microcontroller architectures are beginning to introduce flexibility of ADC implementation through integrated programmable analog capabilities which allow to choose multiple SARs, ΣΔ, and even both simultaneously in the same design. Figure 2 shows the variety of programmable analog components available in such a microcontroller architecture. The analog programmable system allows designers to create application-specific combinations of both standard and advanced analog signal processing blocks. These blocks are then interconnected to each other, providing a high level of design flexibility and IP security.

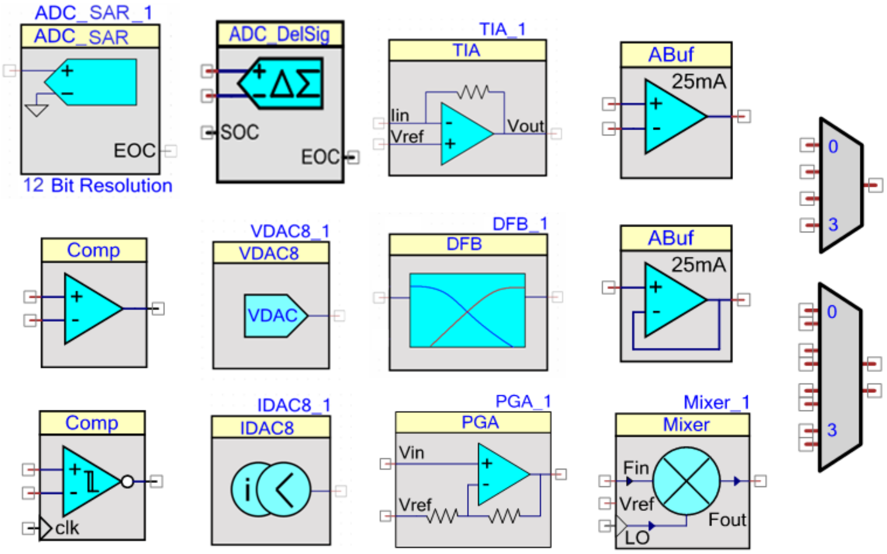

Figure 2: Some of the different analog components available in a programmable analog microcontroller architecture. Designers have the ability to implement the particular components that are best-suited for a particular application.

Using a graphical design editor, developers are able to work in a hardware/software co-design environment to define unique designs. With the ability to configure the analog connections between the GPIO and various analog resources and connections from one analog resource to another, designers can build their own components, such as a SAR ADC that is typically composed of DAC, comparator, and digital logic (see Figure 3).

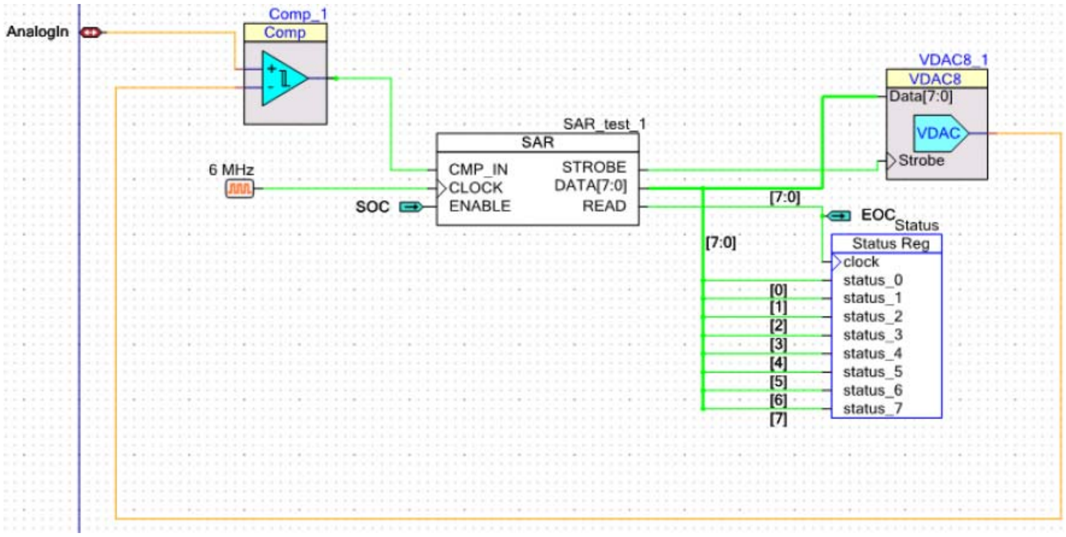

Figure 3: With a flexible hardware/software co-design environment such as Cypress' PSoC Creator, developers can build SAR and ΣΔ ADCs that are optimized for their application.

Programmable analog not only allows flexible and last-minute change development, but also introduces a platform where designers can take a try, make a twist, and manipulate with various discrete analog components in all ranges, and build up the ultimate optimal system no matter which technology is determined to be the Golden Glove Champion.

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