# Cypress Semiconductor
# Product Qualification Report

**QTP# 093606 VERSION 1.0**
**September 2009**

| TrueTouch™ Device Family<br>S4AD-5, Fab4 | |
|---|---|
| CY8CTST110 | TrueTouch™ Single-Touch Touchscreen Controller |

**CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:**


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## PRODUCT QUALIFICATION HISTORY

| Qual Report | | Description of Qualification Purpose | | Date Comp |
|---|---|---|---|---|
| 052004 | | PSoC 8C21001A Neutron Product Family on SONOS S4AD-5 Technology, Fab4 | | Aug 05 |
| 093606 | | Qualify CY8CTST110 Device on S4AD-5 Technology, Fab4 | | Sep 09 |

| PRODUCT DESCRIPTION (for qualification) | |
|---|---|
| Qualification Purpose: CY8CTST110 Device Qualification on S4AD-5 Technology, Fab4 | |
| Marketing Part #: | CY8CTST110 |
| Device Description: | Single-Touch Touchscreen Controller |
| Cypress Division: | Cypress Semiconductor Corporation – Consumer and Computation Division |
| Overall Die (or Mask) REV Level (pre-requisite for qualification): | Rev. A |
| What ID markings on Die: | 8C21001A |

| TECHNOLOGY/FAB PROCESS DESCRIPTION S4AD-5 | | | |
|---|---|---|---|
| Number of Metal Layers: | 2 | Metal Composition: | Metal 1: 500A Ti/6,000A Al 0.5% Cu /1,200A TiW<br>Metal 2: 500A Ti/8,000A Al 0.5% Cu/300A TiW |
| Passivation Type and Materials: | 3,000A TeOs / 6,000A $Si_3N_4$ | | |
| Free Phosphorus contents in top glass layer (%): | 0% | | |
| Number of Transistors in Device: | 100,000 | | |
| Number of Gates in Device | 10,000 | | |
| Generic Process Technology/Design Rule (µ-drawn): | Single Poly, Double Metal, 0.35 µm | | |
| Gate Oxide Material/Thickness (MOS): | $SiO_2$ / 110A | | |
| Name/Location of Die Fab (prime) Facility: | Cypress Semiconductor - Minnesota | | |
| Die Fab Line ID/Wafer Process ID: | Fab 4, S4AD-5 CTI, SONOS | | |

## PACKAGE AVAILABILITY

| PACKAGE | ASSEMBLY SITE FACILITY |
|---|---|
| **56-Lead SSOP** | **CML-RA, PHIL-M, TAIWAN-T** |
| **32-Lead MLF** | **SEOUL-L** |

**Note:** Package Qualification details upon request.

| MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION | |
|---|---|
| **Package Designation:** | SP28 |
| **Package Outline, Type, or Name:** | 28-Lead Shrunk Small Outline Package (SSOP) |
| **Mold Compound Name/Manufacturer:** | Hitachi CEL9220HF |
| **Mold Compound Flammability Rating:** | V-O per UL94 |
| **Oxygen Rating Index:** | >28% |
| **Lead Frame Material:** | Copper |
| **Lead Finish, Composition / Thickness:** | 100% Pure Sn |
| **Die Backside Preparation Method/Metallization:** | Backgrind |
| **Die Separation Method:** | 100% Saw |
| **Die Attach Supplier:** | Ablestik |
| **Die Attach Material:** | 8340 |
| **Die Attach Method:** | Dispensing |
| **Bond Diagram Designation:** | 10-06220 |
| **Wire Bond Method:** | Thermosonic |
| **Wire Material/Size:** | Au, 1.0mil |
| **Thermal Resistance Theta JA °C/W:** | 96°C/W |
| **Package Cross Section Yes/No:** | No |
| **Assembly Process Flow:** | 49-35032 |
| **Name/Location of Assembly (prime) facility:** | OSE Taiwan (TAIWN-T) (28 SSOP) |

| ELECTRICAL TEST / FINISH DESCRIPTION | |
|---|---|
| **Test Location:** | CML-R |
| **Fault Coverage:** | 100% |

**Note:** Please contact a Cypress Representative for other packages availability.

## RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

| Stress/Test | Test Condition<br>(Temp/Bias) | Result<br>P/F |
|---|---|---|
| High Temperature Operating Life<br>Early Failure Rate | Dynamic Operating Condition, Vcc Max=5.5V, 125°C | P |
| High Temperature Operating Life<br>Latent Failure Rate | Dynamic Operating Condition, Vcc Max=5.5V, 125°C | P |
| High Accelerated Saturation Test (HAST) | 130°C, 5.25V, 85%RH<br>Precondition: JESD22 Moisture Sensitivity Level 1<br>168 Hrs, 85C/85%RH+3IR-Reflow, **260°C**+0, -5°C | P |
| Temperature Cycle | MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C<br>Precondition: JESD22 Moisture Sensitivity Level 1<br>168 Hrs, 85C/85%RH+3IR-Reflow, **260°C**+0, -5°C | P |
| Pressure Cooker | 121°C, 100%RH<br>Precondition: JESD22 Moisture Sensitivity Level 1<br>168 Hrs, 85C/85%RH+3IR-Reflow**, 260°C**+0, -5°C | P |
| Data Retention | 150°C ± 5°C No Bias | P |
| High Temperature Steady State life | 125°C, 5.5V, Vcc Max | P |
| Electrostatic Discharge<br>Human Body Model (ESD-HBM) | 2,200V<br>JESD22, Method A114-B | P |
| Electrostatic Discharge<br>Human Body Model (ESD-HBM) | 2,200V<br>MIL-STD-883, Method 3015.7 | P |
| Electrostatic Discharge<br>Charge Device Model (ESD-CDM) | 500V<br>Cypress Spec. 25-00020 | P |
| Endurance Test | MIL-STD-883, Method 883-1033 | P |
| Age Bond Strength | 200C, 4hrs<br>MIL-STD-883, Method 883-2011 | P |
| Current Density | Cypress Spec 22-00029 | P |
| Low Temperature Operating Life | -30C, 5.5V, 8MHZ | P |
| SEM Analysis | MIL-STD-883, Method 883-2018-2 | P |
| Acoustic Microscopy | Spec. 25-00104 | P |
| Dynamic Latch up | 125C, 8.3V | P |
| Latch up Sensitivity | 125C, 11V, ± 300mA<br>In accordance with JEDEC 17. Cypress Spec. 01-00081 | P |

## RELIABILITY FAILURE RATE SUMMARY

| Stress/Test | Device Tested/ Device Hours | # Fails | Activation Energy | Thermal[3] A.F | Failure Rate |
|---|---|---|---|---|---|
| High Temperature Operating Life Early Failure Rate[1] | 3,006 Devices | 0 | N/A | N/A | 0 PPM |
| High Temperature Operating Life[1, 2] Long Term Failure Rate | 528,750 DHRs | 0 | 0 .7 | 55 | 31 FIT |

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate.
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

Where:

$E_A$ =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = $8.62 \times 10^{-5}$ eV/Kelvin.
$T_1$ is the junction temperature of the device under stress and $T_2$ is the junction temperature of the device at use conditions.

# Reliability Test Data

**QTP #: 093606**

| Device | Fab Lot # | Assy Lot # | Assy Loc | Duration | Samp | Rej | Failure Mechanism |
|---|---|---|---|---|---|---|---|
| ***STRESS: ACOUSTIC, MSL1*** | | | | | | | |
| CY8CTST110 | 4516647 | *610521157* | TAIWN-T | COMP | 15 | 0 | |
| CY8CTST110 | 4516674 | *610521849* | PHIL-M | COMP | 15 | 0 | |
| CY8CTST110 | 4517851 | *610522407* | PHIL-M | COMP | 15 | 0 | |
| ***STRESS: AGE BOND STRENGTH*** | | | | | | | |
| CY8CTST110 | 4516647 | *610521157* | TAIWN-T | COMP | 10 | 0 | |
| CY8CTST110 | 4516674 | *610521849* | PHIL-M | COMP | 10 | 0 | |
| CY8CTST110 | 4517851 | *610522407* | PHIL-M | COMP | 10 | 0 | |
| ***STRESS: DATA RETENTION, PLASTIC, 150C*** | | | | | | | |
| CY8CTST110 | 4516647 | *610521157* | TAIWN-T | 500 | 256 | 0 | |
| CY8CTST110 | 4516647 | *610521157* | TAIWN-T | 1000 | 256 | 0 | |
| CY8CTST110 | 4516674 | *610521849* | PHIL-M | 500 | 256 | 0 | |
| CY8CTST110 | 4516674 | *610521849* | PHIL-M | 1000 | 254 | 0 | |
| CY8CTST110 | 4517851 | *610522407* | PHIL-M | 500 | 252 | 0 | |
| CY8CTST110 | 4517851 | *610522407* | PHIL-M | 1000 | 252 | 0 | |
| ***STRESS: ENDURANCE*** | | | | | | | |
| CY8CTST110 | 4516647 | *610521157* | TAIWN-T | COMP | 45 | 0 | |
| ***STRESS: ESD-CHARGE DEVICE MODEL, (500V)*** | | | | | | | |
| CY8CTST110 | 4516647 | *610521157* | TAIWN-T | COMP | 9 | 0 | |
| CY8CTST110 | 4516674 | *610522255* | TAIWN-T | COMP | 9 | 0 | |
| CY8CTST110 | 4517851 | *610522404* | TAIWN-T | COMP | 9 | 0 | |
| ***STRESS: ESD-HUMAN BODY CIRCUIT PER JESD22, METHOD A114-B, (2,200V)*** | | | | | | | |
| CY8CTST110 | 4516647 | *610521157* | TAIWN-T | COMP | 9 | 0 | |
| CY8CTST110 | 4516674 | *610522255* | TAIWN-T | COMP | 9 | 0 | |
| CY8CTST110 | 4517851 | *610522404* | TAIWN-T | COMP | 9 | 0 | |
| ***STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, (2,200V)*** | | | | | | | |
| CY8CTST110 | 4516647 | *610521157* | TAIWN-T | COMP | 3 | 0 | |
| CY8CTST110 | 4516674 | *610522255* | TAIWN-T | COMP | 3 | 0 | |
| CY8CTST110 | 4517851 | *610522404* | TAIWN-T | COMP | 3 | 0 | |

# Reliability Test Data

## QTP #: 093606

| Device | Fab Lot # | Assy Lot # | Assy Loc | Duration | Samp | Rej | Failure Mechanism |
|---|---|---|---|---|---|---|---|
| **STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (125C, 5.5V, Vcc Max)** | | | | | | | |
| CY8CTST110 | 4516647 | *610521157* | TAIWN-T | 120 | 1002 | 0 | |
| CY8CTST110 | 4516674 | *610521849* | PHIL-M | 120 | 1002 | 0 | |
| CY8CTST110 | 4517851 | *610522407* | PHIL-M | 120 | 1002 | 0 | |
| **STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (125C, 5.5V, Vcc Max)** | | | | | | | |
| CY8CTST110 | 4516647 | *610521157* | TAIWN-T | 750 | 235 | 0 | |
| CY8CTST110 | 4517851 | *610522404* | TAIWN-T | 750 | 235 | 0 | |
| CY8CTST110 | 4516674 | *610522255* | TAIWN-T | 750 | 235 | 0 | |
| **STRESS: HIGH TEMP STEADY STATE LIFE TEST (125C, 5.5V)** | | | | | | | |
| CY8CTST110 | 4516647 | *610521157* | TAIWN-T | 168 | 76 | 0 | |
| CY8CTST110 | 4516647 | *610521157* | TAIWN-T | 336 | 76 | 0 | |
| **STRESS: HI-ACCEL SATURATION TEST (130C, 85%RH, 5.25V), PRE CONDITION 168 HR 85C/85%RH (MSL1)** | | | | | | | |
| CY8CTST110 | 4516647 | *610527569* | PHIL-M | 128 | 49 | 0 | |
| CY8CTST110 | 4516674 | *610521849* | PHIL-M | 128 | 44 | 0 | |
| CY8CTST110 | 4517851 | *610522407* | PHIL-M | 128 | 44 | 0 | |
| **STRESS: LOW TEMPERATURE OPERATING LIFE (-30C, 5.5V)** | | | | | | | |
| CY8CTST110 | 4516647 | *610521157* | TAIWN-T | 500 | 45 | 0 | |
| **STRESS: PRESSURE COOKER TEST (121C, 100%RH), PRE CONDITION 168 HR 85C/85%RH (MSL1)** | | | | | | | |
| CY8CTST110 | 4516647 | *610521157* | TAIWN-T | 168 | 45 | 0 | |
| CY8CTST110 | 4516647 | *610521157* | TAIWN-T | 336 | 45 | 0 | |
| CY8CTST110 | 4516674 | *610521849* | PHIL-M | 168 | 45 | 0 | |
| CY8CTST110 | 4516674 | *610521849* | PHIL-M | 336 | 45 | 0 | |
| CY8CTST110 | 4517851 | *610522407* | PHIL-M | 168 | 45 | 0 | |
| CY8CTST110 | 4517851 | *610522407* | PHIL-M | 336 | 45 | 0 | |
| **STRESS: STATIC LATCH-UP TESTING (125C, 11V, ±300mA)** | | | | | | | |
| CY8CTST110 | 4516647 | *610521157* | TAIWN-T | COMP | 3 | 0 | |
| CY8CTST110 | 4516674 | *610522255* | TAIWN-T | COMP | 3 | 0 | |
| CY8CTST110 | 4517851 | *610522404* | TAIWN-T | COMP | 3 | 0 | |
| **STRESS: DYNAMIC LATCH-UP (8.3V)** | | | | | | | |
| CY8CTST110 | 4516647 | *610521157* | TAIWN-T | COMP | 3 | 0 | |

# Reliability Test Data

**QTP #: 093606**

| Device | Fab Lot # | Assy Lot # | Assy Loc | Duration | Samp | Rej | Failure Mechanism |
|---|---|---|---|---|---|---|---|
| ***STRESS: TC COND. C -65C TO 150C, PRECONDITION 168 HRS 85C/85%RH (MSL1)*** | | | | | | | |
| CY8CTST110 | 4516647 | *610521157* | TAIWN-T | 300 | 50 | 0 | |
| CY8CTST110 | 4516647 | *610521157* | TAIWN-T | 500 | 50 | 0 | |
| CY8CTST110 | 4516647 | *610521157* | TAIWN-T | 1000 | 50 | 0 | |
| CY8CTST110 | 4516674 | *610521849* | PHIL-M | 300 | 45 | 0 | |
| CY8CTST110 | 4516674 | *610521849* | PHIL-M | 1000 | 45 | 0 | |
| CY8CTST110 | 4517851 | *610522407* | PHIL-M | 300 | 45 | 0 | |