Efficient Design of a Brushless DC Fan with a Programmable System-on-a-Chip

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As more industrial and consumer products get smaller, the need to remove the heat in an efficient, quiet way becomes increasingly important. A programmable system on a chip produces an efficient, cost-effective means for accomplishing this.

A typical intelligent DC fan (see Figure 1) has four wires; power (**red**), ground (**black**), a PWM input to set fan speed (**blue**), and a tachometer output (**green**). The host system requests a specific speed by setting the duty cycle of the PWM and verifies the correct operation with the tachometer feedback. Measuring the ambient temperature allows the fan to run as slow and as seldom as possible. It comes at the cost of a thermistor.

To reduce mechanical noise and increase operation lifetime, this design example will control a single-phase, 4-pole brushless DC motor. A fan motor is a unique design with a 4-pole permanent magnet rotor on the outside and a stationary 4-pole stator. The poles are alternately wound in series resulting in a single coil. Applying a current to the coil in one direction will lock the motor at either 0º or 180º. Applying current the opposite direction will lock the motor at 90º or 270º. With an analog Hall effect sensor to measure the rotor position, developers can adjust the magnitude and current direction to control the motors rotation.

This coil is driven with a 4-transistor H bridge to control current direction and the appropriate leg is driven with a PWM to set the current magnitude. A current shunt is added to monitor the coil current.

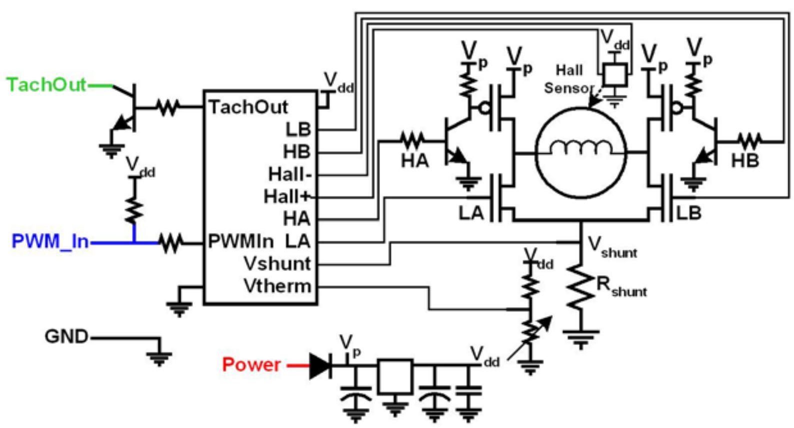

Figure 1: Schematic for the Specified Four Wire Fan

This fan is required to operate from 600 rpm to 30,000 rpm, well within the capacity of a microcontroller assisted with analog and digital peripherals to control and an ideal application for a microcontroller-based programmable system-on-a-chip. The following peripherals are required:

- A **comparator** to convert the differential analog outputs of the Hall sensor into a digital signal.
- An **8-bit PWM** to control the magnitude of the coil current. To control the current's direction, the microcontroller switches the PWM into the appropriate lower leg of the FET bridge. The PWM output frequency is set to 23.4kHz (6MHz/256), just above the human audio range
- A **16-bit timer** to measure the edges from the Hall sensor comparator. This timer will measure the time for all four phases of the motor because the four poles are not perfectly spaced. The timing for each pole is needed because driving the coil for the very last bit of each cycle does not produce any significant power while consuming a significant amount of current. To conserve power, the PWM is stopped some empirically determined amount of time before the end of the cycle. The PWM uses the previous known phase time to turn itself off early.
- A **16-bit timer** to measure the duty cycle to the incoming speed selection control signal. The timer is clocked at 24 MHz. The timer is set to measure the time for a falling edge, the next raising edge, and the next falling edge. The duty cycle is shown in the equation:

$$DutyCycle = \frac{\frac{n_r - n_{f2}}{f_{clk}}}{\frac{n_{f1} - n_{f2}}{f_{clk}}} = \frac{n_r - n_{f2}}{n_r - n_{f2}}$$

- Note that clock accuracy falls out of the equation. For example, a 24 MHz timer clocking a 25 kHz input has a period of 960 with accuracy much less than 0.2%.
- An **ADC** to measure the shunt current and thermistor voltages.

A Cypress **CY8C21323-24LFXI** PSoC programmable system-on-a-chip is selected to control this design. It comes in a 24-pin MLF package, contains a microcontroller, and has the following peripherals:

- **Four 8-bit Digital blocks** that can be configured to be timers, counters, and PWMs. They can be cascaded to make wider peripherals.
- **Two Analog blocks** that can be used as single-ended, programmable comparators. Combine one with a properly configured digital block and you have a 10-bit ADC. Both of these blocks can be combined into a comparator with differential inputs.

At first glance it appears that there are not enough peripherals to construct the required system elements. As Figure 2 below shows, if the control is segmented into eight different states, many of the required elements can share the available system resources.

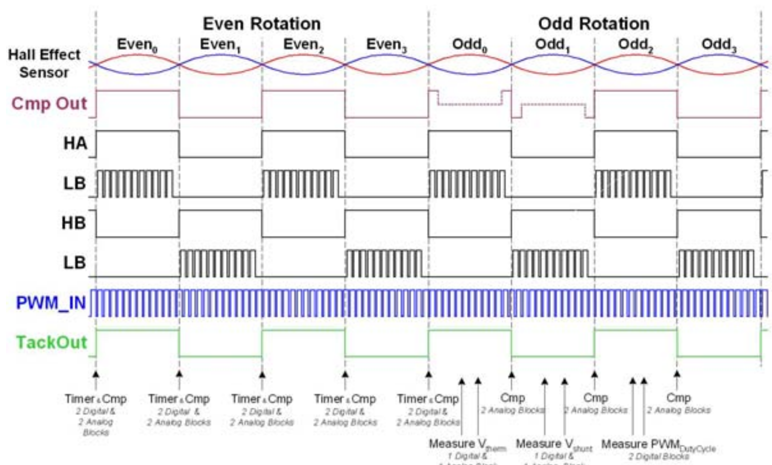

Figure 2: Timing Diagram for Dynamically Reconfigured 4 Wire Fan

The timing is broken down into two rotations with each rotation having four phases. The PWM is required for all eight phases, so it cannot be shared and requires a single digital block. Each phase starts with the transition on the Hall sensor, comprised of two analog blocks. At this point, all the FETs are turned off and the appropriate high-side FET is turned on. The PWM is connected to the appropriate low-side FET and is turned on. The PWM uses the previously calculated speed to determine when to turn itself off.

From just before the end of **Odd$_3$** to the just after the start of **Odd$_0$**, two of the digital blocks are configured to make a 16-bit timer and measure the four even phase widths. This information is used to calculate the fan speed. Note that the speed is not measured for odd rotations.

In the middle of **Odd$_0$**, one analog block and one digital block are reconfigured to build an ADC and measure the shunt current. After finishing, the analog blocks are reconfigured to rebuild the Hall comparator. The same is done in **Odd$_1$** to measure the thermistor voltage. In **Odd3,** two digital blocks are reconfigured to measure the duty cycle of the incoming PWM. When finished, they are reconfigured to measure fan speed, and the cycle repeats.

With this configuration, only three of the digital blocks are used. The fourth is available for additional free features.

A programmable system-on-a-chip allows for reduced components and performance improvements. Dynamic reconfiguration allows for the sharing of system resources as well as reducing system cost.

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