CYPRESS

2000 Q4 RELIABILITY REPORT

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Note: All the results reported here are for Quarter 4 2000.

CYPRESS

1.0 OVERVIEW OF CYPRESS SEMICONDUCTOR TOTAL QUALITY MANAGEMENT SYSTEM

This report summarizes Cypress Semiconductor Product Reliability for the 4th quarter of 2000. Cypress Semiconductor has established aggressive reliability objectives to assure that all products exhibit reliability which exceeds customer reliability requirements for purchased components. In addition, the quality standard at Cypress is zero defects which results in a culture requiring continuous improvement in quality and reliability. This report includes data from product fabricated at the San Jose, California; Round Rock, Texas; and Bloomington, Minnesota facilities. Product reliability is assured by a total quality management system. The quality management system is described in detail in the Cypress Semiconductor Quality Manual (Cypress Semiconductor Document Number 90-00001). Key reliability-related programs of the total quality management system are: (1) design rule review and approval; (2) control of raw materials and vendor quality; (3) manufacturing statistical process controls; (4) manufacturing identification of "Maverick Lot" yield limits; (5) formal training and certification of manufacturing personnel; (6) qualification of new products and manufacturing processes; (7) continuous reliability monitoring; (8) formal failure analysis and corrective action; and (9) competitive benchmarking. Product Reliability data is accumulated as a result of new product Qualification Test Plan activities (Cypress Semiconductor Document Number 25-00040) as well as from the Reliability Monitor Program (Cypress Semiconductor Document Number 25-00008). All reliability test samples are obtained from standard production material. Sample selection is based on generic product families. These generic products are designed with very similar design rules and manufactured from a core set of processes. Reliability strategy requires that every failure which occurs during reliability testing be subjected to failure analysis (Cypress Semiconductor Document Number 25-00039) to determine the failure mechanism. Corrective action is then implemented to prevent future failures. The result is continuous improvement in product reliability. Copies of the Cypress Semiconductor documents referenced herein are available through your Cypress Semiconductor sales representative. Questions about product reliability may be addressed to the undersigned.

Director of Reliability   Director of Quality

Cypress Semiconductor Corporation
3901 North First Street
San Jose, CA 95134-1599
Cypress Quality Fax: (408) 943-2165

2.0 EARLY FAILURE RATE SUMMARY

2.1 Early Failure Rate Determination High Temperature Operating Life testing (HTOL), for as long as 96 hours, is used to estimate device early failure rate. This stress test will typically correspond to the first 2000 hours of device operation in a system environment.

Test: High Temperature Operating Life Test (HTOL)
Conditions: Dynamic Operating Conditions, VCC up to VCC, nominal + 15%, 150°C or 125°C.
Duration: Early Failure Rate samples are tested between 48 hours HTOL at 150°C (EFR) or 96 hours at 125°C (EFR2).
Failure: A failure is any device that fails to meet data sheet electrical requirements.
Fit Rate: Derated to 55 c ambient, with 60% upper confidence bound for 0 failures, Ea =0.7ev

Early Failure Rate Summary

Technology	Device Hours	# Failed	FIT Rate	Failure Mode
HYNIX P26	149376	0	36.1	None
P26	219530	0	24.6	None
Ram 2	501092	1	11.7	
Ram 4	3201843	6	11.0	Single bit, ISB
Ram 5	4812142	10	12.2	Particle defect
TSMC L28	178944	0	30.1	None

Note: Data reported is a 4 quarter rolling average.

3.0 LONG TERM FAILURE RATE SUMMARY

3.1 Long Term Failure Rate Determination
A High Temperature Operating Life test (HTOL) is used to estimate long term reliability. By operating the devices at accelerated temperature and voltage, hundreds of thousands of use hours can be compressed into hundreds of test hours.

Test: High Temperature Operating Life Test (HTOL)
Conditions: Dynamic Operating Conditions, VCC up to VCC, nominal + 15% 150°C or 125°C
Duration: A minimum of 80 hours at 150°C or 168 hours at125°C. Tested to 500 hours at 150°C or 1000 hours at 125°C.
Failure: A failure is any device that fails to meet data sheet electrical requirements.
Fit Rate: Derated to 55 c ambient, with 60% upper confidence bound for 0 failures, Ea =0.7ev

Long Term Failure Rate Summary

Technology	Device Hours @150°C	# Failed	FIT Rate	Failure Mode
CMOS	115500	0	46.7	None
FL28	164400	0	32.8	None
HYNIX 0.35	226160	0	23.8	None
HYNIX P26	258480	0	20.9	None

P20	86500	0	62.3	None
P26	117371	0	45.9	None
Ram 2	1087860	2	10.8	Cause not known
Ram 3	649120	2	18.1	Cause not known
Ram 4	2135087	1	2.8	Cause not known
Ram 5	3001919	7	13.7	Particle contamination and poly defects in fab
TSMC 0.5	234316	0	23.0	None
TSMC L28	171240	0	31.5	None

Note: Data reported is a 4 quarter rolling average.

4.0 PROCESS ENVIRONMENTAL TESTS

Cypress Semiconductor Reliability qualifies and continuously monitors packaging reliability to ensure exceptional resistance to environmental stress. Package reliability stress testing and failure rates are summarized in the following section.

4.1 Pressure Cooker Test (PCT)

Test: Pressure Cooker Test (PCT)

Conditions: 15 PSIG, 121°C, No bias, for a minimum of 168 hours.

Pre-Conditioning: 5 cycles Temperature Cycles –65/+150, 24 hr Bake 125°C, Moisture loading to qualified MSL level

Purpose: The Pressure Cooker Test is a highly accelerated packaging stress test used to ensure environmental durability of epoxy packaged parts. Passivation cracks, ionic contamination and corrosion susceptibility are all accelerated by this stress.

Failure: A failure is any device that fails to meet data sheet electrical requirements.

Pressure Cooker Test Failure Rate Summary

Package	Sample Size	# Failed	Defects %	Failure Mode
TQFP	2045	0	0	None
PPGA	893	0	0	None
PLCC	2306	0	0	None
PQFP	278	0	0	None
PDIP	725	0	0	None
SSOP	657	0	0	None
SOIC	1750	0	0	None
SOJ	1961	0	0	None
TSOP	1435	0	0	None

Note: Data reported is a 4 quarter rolling average.

4.2 Highly Accelerated Stress Test (HAST)

Cypress uses HAST to accelerate temperature, humidity, bias failure mechanisms. This change was necessary because our package reliability had improved to the point where the old 85°C/85% R.H. temperature-humidity-bias testing would not induce failures. Failures are necessary to judge progress and compare packaging changes. HAST testing has been shown to be at least twenty times more accelerated then 85°C/85% R.H. temperature-humidity-bias testing.

Test: Highly Accelerated Stress Test (HAST)
Conditions: Present Conditions: 130°C / 85% RH minimum power dissipation, for a minimum of 128 hours.
Pre-Conditioning: 5 cycles Temperature Cycles –65/+150, 24 hr Bake 125°C, Moisture loading to qualified MSL level
Purpose: HAST is an accelerated biased humidity test that provides an acceleration of at least 20 over 85°C/85% R.H. temperature-humidity bias testing. This test provides rapid feedback regarding the quality of the epoxy package process.
Failure: A failure is any device that fails to meet data sheet electrical requirements.

Highly Accelerated Stress Test (HAST) Failure Rate Summary

Package	Sample Size	# Failed	Defects %	Failure Mode
TQFP	1128	0	0	None
PPGA	775	0	0	None
PLCC	1024	0	0	None
PQFP	149	0	0	None
PDIP	135	0	0	None
SSOP	599	0	0	None
SOIC	1242	3	0.2	Lifted Bond
SOJ	1644	0	0	None
TSOP	933	0	0	None

Note: Data reported is a 4 quarter rolling average.

4.3 Temperature Cycle Test (TC)

Differences in thermal expansion coefficients are accentuated by cycling devices through temperature extremes. If the materials do not expand and contract equally, large stresses can develop.

Test: Temperature Cycle
Condition: MIL-STD-883D, Method 1010, Condition C, -65°C to 150°C.
JEDEC 22-A104 Condition B, -40°C to 125°C
Pre-Condition: 5 cycles Temperature Cycles –65/+150, 24 hr Bake 125°C, Moisture loading to qualified MSL level
Purpose: The Temperature Cycle test stresses mechanical integrity by exposing a device to alternating temperature extremes. Weakness and thermal expansion mismatches in die interconnections, die attach, and wire bonds are often detected with this acceleration test.
Duration: 300 cycles minimum at Condition C, minimum 1000 cycles at Condition B.
Failure: A failure is any device that fails to meet data sheet electrical requirements.

Temperature Cycling Failure Rate Summary

Package	Sample Size	# Failed	Defects %	Failure Mode
TQFP	2700	3	0.04	Dielectric crack
PPGA	2188	0	0	None
PLCC	1527	0	0	None
PQFP	374	0	0	None
PDIP	365	0	0	None
SSOP	992	0	0	None
SOIC	1958	0	0	None
SOJ	2667	0	0	None
TSOP	1586	0	0	None

Note: Data reported is a 4 quarter rolling average.