2000 Q2 RELIABILITY REPORT

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Note: All the results reported here are for Quarter 2 2000.

1.0 OVERVIEW OF CYPRESS SEMICONDUCTOR TOTAL QUALITY MANAGEMENT SYSTEM

This report summarizes Cypress Semiconductor Product Reliability for the 2nd quarter of 2000. Cypress Semiconductor has established aggressive reliability objectives to assure that all products exhibit reliability which exceeds customer reliability requirements for purchased components. In addition, the quality standard at Cypress is zero defects which results in a culture requiring continuous improvement in quality and reliability. This report includes data from product fabricated at the San Jose, California; Round Rock, Texas; and Bloomington, Minnesota facilities. Product reliability is assured by a total quality management system. The quality management system is described in detail in the Cypress Semiconductor Quality Manual (Cypress Semiconductor Document Number 90-00001). Key reliability-related programs of the total quality management system are: (1) design rule review and approval; (2) control of raw materials and vendor quality; (3) manufacturing statistical process controls; (4) manufacturing identification of "Maverick Lot" yield limits; (5) formal training and certification of manufacturing personnel; (6) qualification of new products and manufacturing processes; (7) continuous reliability monitoring; (8) formal failure analysis and corrective action; and (9) competitive benchmarking. Product Reliability data is accumulated as a result of new product Qualification Test Plan activities (Cypress Semiconductor Document Number 25-00040) as well as from the Reliability Monitor Program (Cypress Semiconductor Document Number 25-00008). All reliability test samples are obtained from standard production material. Sample selection is based on generic product families. These generic products are designed with very similar design rules and manufactured from a core set of processes. Reliability strategy requires that every failure which occurs during reliability testing be subjected to failure analysis (Cypress Semiconductor Document Number 25-00039) to determine the failure mechanism. Corrective action is then implemented to prevent future failures. The result is continuous improvement in product reliability. Copies of the Cypress Semiconductor documents referenced herein are available through your Cypress Semiconductor sales representative. Questions about product reliability may be addressed to the undersigned.

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2.0 EARLY FAILURE RATE SUMMARY

2.1 Early Failure Rate Determination High Temperature Operating Life testing (HTOL), for as long as 96 hours, is used to estimate device early failure rate.

Test: High Temperature Operating Life Test (HTOL)
Conditions: Dynamic Operating Conditions, VCC up to VCC, nominal + 15%, 150°C or 125°C.
Duration: Early Failure Rate samples are tested between 48 hours HTOL at 150°C (EFR) or up to 96 hours at 125°C (EFR2).
Failure: A failure is any device that fails to meet data sheet electrical requirements.
Fit Rate: Derated to 55° C ambient, with 60% upper confidence bound for 0 failures, Ea =0.7ev

Early Failure Rate Summary

Technology	Device hours	# Failed	FIT Rate	Failure Mode
Hynix P26	100992	0	53.4	None
P26	449904	0	12	None
Ram 2	1605192	0	3.4	None
Ram 3	262538	0		None
Ram 4	4206978	5	7	Particle Defect, Single bit
Ram 5	3738918	11	17.3	Poly particle defect, Single bit
TSMC L28	178944	0	30.1	None

Note: Data reported is a 4 quarter rolling average.

3.0 LONG TERM FAILURE RATE SUMMARY

3.1 Long Term Failure Rate Determination
A High Temperature Operating Life test (HTOL) is used to estimate long term reliability. By operating the devices at accelerated temperature and voltage, hundreds of thousands of use hours can be compressed into hundreds of test hours.

Test: High Temperature Operating Life Test (HTOL)
Conditions: Dynamic Operating Conditions, VCC up to VCC, nominal + 15% 150°C or 125°C
Duration: A minimum of 80 hours at 150°C or 168 hours at 125°C. Tested to 500 hours at 150°C or 1000 hours at 125°C.
Failure: A failure is any device that fails to meet data sheet electrical requirements.
Fit Rate: Derated to 55° C ambient, with 60% upper confidence bound for 0 failures, Ea =0.7ev

Long Term Failure Rate Summary

Technology	Device Hours @150°c	# Failed	FIT	Failure Mode
CMOS	115000	0	46.7	None
FL28	141896	0	38	None
HYNIX 0.35	226160	0	23.8	None

HYNIX P26	258480	0	20.9	None
P20	154300	0	34.9	None
P26	69600	0	77.4	None
Ram 2	1156536	2	10.2	EOS
Ram 3	1132432	2	10.4	EOS
Ram 4	2326998	2	5.1	Single bit
Ram 5	4767403	11	13.6	Particle contamination and poly defects in fab,
TSMC 0.5	58320	0	92.4	None
TSMC L28	171240	0	31.5	None

Note: Data reported is a 4 quarter rolling average.

4.0 PROCESS ENVIRONMENTAL TESTS

Cypress Semiconductor Reliability qualifies and continuously monitors packaging reliability to ensure exceptional resistance to environmental stress. Package reliability stress testing and failure rates are summarized in the following section.

4.1 Pressure Cooker Test (PCT)

Test: Pressure Cooker Test (PCT)

Conditions: 15 PSIG, 121°C, No bias, for a minimum of 168 hours.

Pre-Conditioning: 5 cycles Temperature Cycles –65/+150, 24 hr Bake 125°C, Moisture loading to qualified MSL level

Purpose: The Pressure Cooker Test is a highly accelerated packaging stress test used to ensure environmental durability of epoxy packaged parts. Passivation cracks, ionic contamination and corrosion susceptibility are all accelerated by this stress.

Failure: A failure is any device that fails to meet data sheet electrical requirements.

Pressure Cooker Test Failure Rate Summary

Package	Sample Size	# Failed	Defects %	Failure Mode
TQFP	2488	0	0	None
PPGA	849	0	0	None
PLCC	2219	4	0.18	Corrosion
PQFP	280	0	0	None
PDIP	446	0	0	None
SSOP	865	0	0	None
SOIC	1165	3	0.25	Wedge Cut
SOJ	1513	0	0	None
TSOP	1282	0	0	None

Note: Data reported is a 4 quarter rolling average.

4.2 Highly Accelerated Stress Test (HAST)

Cypress uses HAST to accelerate temperature, humidity, bias failure mechanisms. This change was necessary because our package reliability had improved to the point where the old 85°C/85% R.H.

temperature-humidity-bias testing would not induce failures. Failures are necessary to judge progress and compare packaging changes. HAST testing has been shown to be at least twenty times more accelerated then 85°C/85% R.H. temperature-humidity-bias testing.

Test: Highly Accelerated Stress Test (HAST)
Conditions: Present Conditions: 130°C / 85% minimum power dissipation, for a minimum of 128 hours.
Pre-Conditioning: 5 cycles Temperature Cycles –65/+150, 24 hr Bake 125°C, Moisture loading to qualified MSL level
Purpose: HAST is an accelerated biased humidity test that provides an acceleration of at least 20 over 85°C/85% R.H. temperature-humidity bias testing. This test provides rapid feedback regarding the quality of the epoxy package process.
Failure: A failure is any device that fails to meet data sheet electrical requirements.

Highly Accelerated Stress Test (HAST) Failure Rate Summary

Package	Sample Size	Failure	Defects %	Failure Mode
TQFP	1199	0	0	None
PPGA	695	0	0	None
PLCC	1245	0	0	None
PQFP	149	0	0	None
PDIP	45	0	0	None
SSOP	526	0	0	None
SOIC	794	0	0	None
SOJ	1513	1	0.06	Lifted ball bond
TSOP	223	1	0.12	Corroded metallization

Note: Data reported is a 4 quarter rolling average.

4.3 Temperature Cycle Test (TC)

Differences in thermal expansion coefficients are accentuated by cycling devices through temperature extremes. If the materials do not expand and contract equally, large stresses can develop.

Test: Temperature Cycle
Condition: MIL-STD-883D, Method 1010, Condition C, -65°C to 150°C.
JEDEC 22-A104 Condition B, -40°C to 125°C
Pre-Condition: 5 cycles Temperature Cycles –65/+150, 24 hr Bake 125°C, Moisture loading to qualified MSL level
Purpose: The Temperature Cycle test stresses mechanical integrity by exposing a device to alternating temperature extremes. Weakness and thermal expansion mismatches in die interconnections, die attach, and wire bonds are often detected with this acceleration test.
Duration: 300 cycles minimum at Condition C, 1000 cycles at Condtion B
Failure: A failure is any device that fails to meet data sheet electrical requirements.

Temperature Cycling Failure Rate Summary

Package	Sample Size	# Failed	Defects %	Failure Mode
TQFP	2463	2	0.08	Wedge cut
PPGA	2279	0	0	None
PLCC	1892	0	0	None
PDIP	319	1	0.31	Top side crack
PQFP	374	0	0	None
SSOP	1030	0	0	None
SOIC	1208	0	0	None
SOJ	2428	0	0	None
TSOP	2314	0	0	None

Note: Data reported is a 4 quarter rolling average.