Using Delta-Sigma Can Be As Easy As ADC (Part 5)

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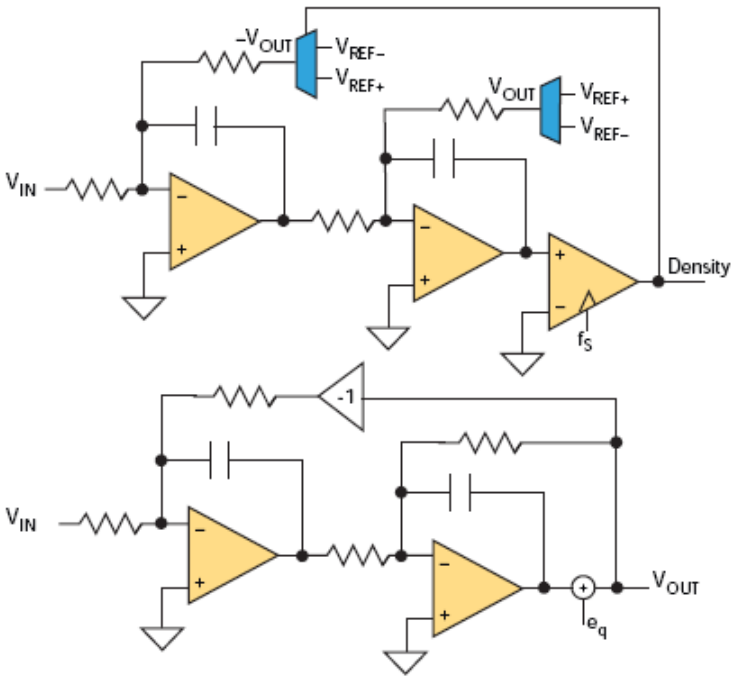
Part 4 of this series showed how a single-stage delta-sigma modulator (DSM) produces an output that is a sum of the low pass-filtered input signal and the high pass-filtered quantization noise. The primary difference between a filter and a DSM is that a filter feeds back its output while the DSM feeds back its quantized output. If this is all you take away from this series of columns, it is enough to justify my effort.

The high pass filtering of the quantization noise pushes it to a higher frequency, allowing easier removal with a decimation filter. Reducing the filter bandwidth by a factor of four (two octaves) decreases the noise by a factor of eight, or 18 dB (*Equation 1*):

$$\eta_0 = \sqrt{\frac{2}{3}} \times e_{RMS}2 \times \left(\frac{f_0}{f_S}\right)^{\frac{3}{2}}$$

The noise reduction is 9 dB per octave. And as with filters, if you need more performance, you just increase the number of sections. If a single-pole filter isn't adequate, make it two, three, or more poles. The same goes for DSMs (*Fig 1*).



1. For more performance in delta-sigma modulators like this second-order example, simply increase the number of sections.

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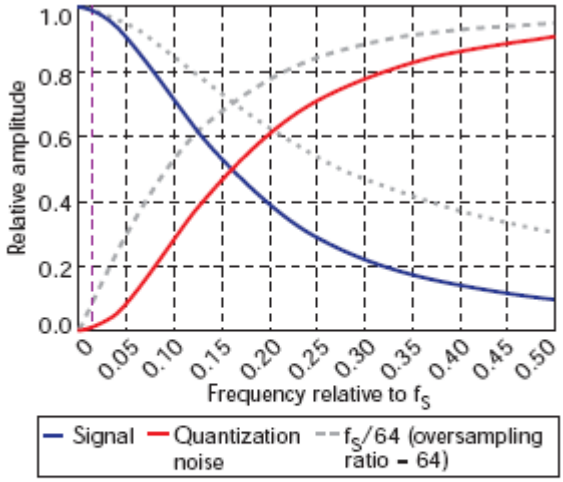
If the quantization circuitry were removed, it would be an ordinary two-pole low pass filter. When we add the quantization hardware, the output becomes the sum of the low passed-filtered input signal and the high passed-filtered quantization noise. Setting the RC time constant to match that of the sample clock ($RC = 1/f_S$) results in Equation 2, relating the output voltage to the input signal and quantization error:

$$V_{OUT} = V_{IN} \times \frac{1}{\left(1+\frac{s}{f_S}\right)^2} + e_q \frac{\left(\frac{s}{f_S}\right)^2}{\left(1+\frac{s}{f_S}\right)^2}$$

As with the first-order modulator, the output is a sum of the low pass-filtered input signal and the high pass-filtered quantization noise. But with the second-order modulators, the rolloff is enhanced. The relative amplitude of both the signal and the quantization noise can be plotted as a function of frequency (*Fig. 2*).



2. In second-order DSMs, the relative amplitude of the signal and quantization noise can be plotted as a function of frequency.

Along with the quantization plot, the single-order DSM quantization is added to show the difference in the noise spreading. The plot shows that the quantization noise has been pushed (shaped) further toward the higher end of the spectrum. At a fairly low frequency, its relative response is roughly parabolic. Equation 3 shows the response:

$$\eta(f) \quad \frac{e_{RMS}}{\sqrt{\frac{f_S}{2}}} \times \left(\frac{2\ f}{f_S}\right)^2 ; f << f_S$$

sample rate (f_0). The amount of noise below this value is even smaller than with a single-order DSM. To calculate the total quantization noise, each bit of the noise left in this band must be added (Equation 4):

$$\eta_0 = \sqrt{\int_0^{f_0} \eta(f)^2 \, df} \approx \sqrt{\frac{2}{5}} \times e_{RMS}(2\ \ )^2 \left(\frac{f_0}{f_S}\right); f_0 << f_S$$

A reduction of two octaves reduces the in-band quantization noise by 30 dB. With the proper filter, it is possible to achieve 15 dB/octave. For a second-order modulator with a 1-Msample/s clock and the proper decimator, it is possible to get 16-bit resolution at 7.8 ksamples/s. This is better than the 488 samples/s for the single-order DSM obtained in Part 4 of this series of columns.

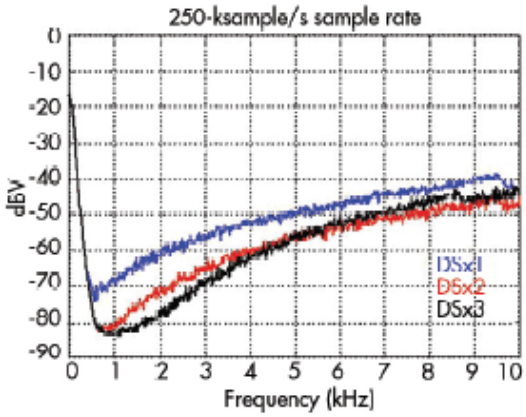
EVEN HIGHER-ORDER DSMs

Just like filters, higher-order modulators can be built with the addition of integrators and quantization feedback. An "L" order modulator will have "L" integrators and "L" feedback loops. (L is for loop.) It also will have the following band noise (Equation 5):

$$\eta_0 \quad \sqrt{\frac{2}{2L+1}} \times e_{RMS}(2\ \ )^L \left(\frac{f_0}{f_S}\right)^{\frac{2L+1}{2}}; f_0 << f_S$$

The noise reduction will be 21 dB/octave for a third-order modulator, 27 dB/octave for a fourth-order module, and so on. Given a 1-Msample clock, a third-order modulator with the correct decimator will result in 16-bit resolution at 25 ksamples/s. A fourth-order modulator should have the same resolution at 50 ksamples/s.

Developing practical higher-order modulators isn't an easy task. As with filters, practical designs come with experience. My goal in writing this series has been to show how delta-sigma modulators operate. This way, when you see a data sheet for a part with a sixth-order DSM, you will understand that its resolution enhancement is 39 dB/octave and how it is possible to get so much resolution with such a relatively small system clock. For real examples, I built first-, second-, and third-order delta-sigma modulators, each with a 250-ksample/s clock. They were constructed using a Cypress CY8C27443 programmable system on a chip. The input was a 100-Hz sinusoid, and the digital output was fed to a Hewlett-Packard 3585A spectrum analyzer. Figure 3 shows the results for the three difference modulators. It is apparent that the noise gets lower as the modulation order increases.



3. Noise decreases as modulation order increases from first- to second- and then third-order DSMs.

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SUMMARY

Delta-sigma modulation appears complicated, but it can be made easier to understand viewed from a historical perspective. By starting with single-slope converters and moving to dual-slope, single- stage DSMs, and finally to multi-order DSMs, the motivations for each increment becomes apparent in how each improved performance and reduced cost. No grand plan. No intrinsic beauty. Just simple engineering practices applied over time.

For those interested in building their own DSMs, I have projects for single-, dual-, and triple-order modulators. These projects work with the chip earlier discussed.

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