Using Delta-Sigma Can Be As Easy As ADC (Part 4)

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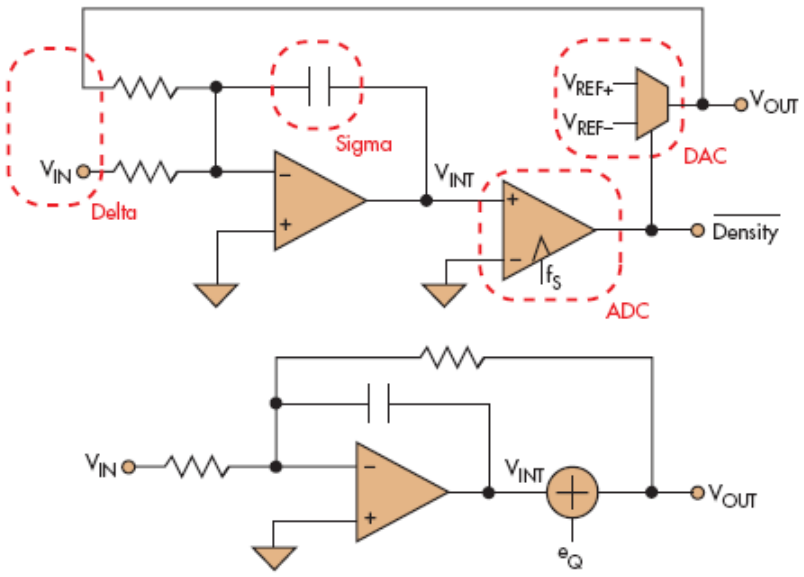
Based on the amount of e-mail I received after Part 3 of this series, many of you have already guessed that an incremental integrator is really just a delta-sigma modulator (DSM). Well, you're right! It actually is a continuous-time delta-sigma modulator. "Continuous time" comes from the fact that the integrator comprises resistors, a capacitor, and an op amp.

Most commercial DSMs are made with switched capacitor technology. I decided to explain continuous time because most engineers that are unfamiliar with DSM theory are more comfortable with linear circuits and Laplace transforms than they are with switched capacitors and z transforms. Switched capacitors will be a subject for a future column.

THE DETAILS

A DSM must have a difference (delta) circuit, an integrate or accumulate (sigma) circuit, and a quantization (modulation) circuit consisting of an ADC and a DAC. Figure 1 shows that the increment integrator is a DSM. The op-amp feedback causes the quantized output to be subtracted (?) from the input, and the result is integrated (S). The comparator on the output serves as a singlebit ADC and is the density output. This digital output controls the reference MUX, serving as a single DAC, resulting in a quantized (M) feedback signal.

1. In this DSM, the op-amp feedback causes the quantized output to be subtracted from the input, and the result is integrated.



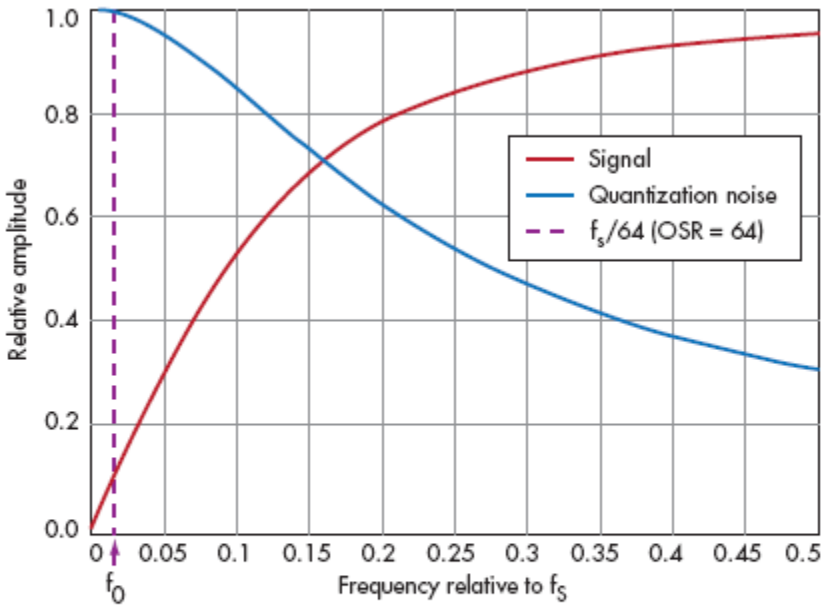
Suppose the references are ±1 V. A 0.1-V integrator output results in a 1-V quantized output. This can be seen as 0.1 V with a 0.9 quantization error. A quantized –0.3 is –1 V or the addition of a –0.7-V quantization error. Bearing this in mind, a DSM can be considered an integrator with a quantization noise source added to its output. Figure 1 shows this model of quantization noise.

Setting the RC time constant to match that of the sample clock ($RC = 1/f_S$) results in Equation 1, relating the output voltage to the input signal and quantization error:

Published in Electronic Design (http://electronicdesign.com/Articles/ArticleID/20485/20485.html) January 2009

$$V_{OUT} = -V_{IN} \times \frac{1}{1+\frac{s}{f_S}} + e_Q \frac{\frac{s}{f_S}}{1+\frac{s}{f_S}}$$

The output is the sum of the low pass filtered input signal and the high pass filtered quantization noise. The relative amplitude of each is plotted as a function of frequency (*Fig. 2*). The plot clearly shows that the quantization noise has been pushed (shaped) toward the higher end of the spectrum. At a fairly low frequency, its relative response is roughly linear (*Equation 2*):



2. As a DSM's noise frequency relative to f_S increases, the quantization noise's relative amplitude increases, while the signal's relative amplitude decreases.

$$n(f) \approx \frac{e_{rms}}{\sqrt{\frac{f_S}{2}}} \times \frac{2\pi f}{f_S}; f << f_S$$

The lower the frequency, the less quantization noise there is. The plot has a marker set to some frequency far less than the sample rate (f_0). The amount of noise below that value is small, and the signal to noise ratio (SNR) is large. Making the bandwidth smaller increases the SNR ratio. To calculate the total quantization noise, each bit of the noise left in this band must be added (*Equation 3*):

$$\eta_0 = \sqrt{\int_0^{f_0} \eta(f)^2 \, df} \approx \sqrt{\frac{8}{3}\pi} \times e_{rms} \times \left(\frac{f_s}{f_0}\right)^{\frac{3}{2}} = \sqrt{\frac{8}{3}\pi} \times e_{rms} \times OSR^{-\frac{3}{2}}; \; f << f_s$$

The noise is accumulated using root square sum. Note that the total noise is inversely proportional to $f_0^{3/2}$. Lower the bandwidth by two octaves (12 dB), and the noise goes down by a factor of eight (18 dB). With the proper digital filter, it is possible to achieve 9-dB/octave performance from such a delta-sigma modulator.

The proper filter is called a decimator. The word “decimate” is Roman in origin, meaning to reduce by a tenth. Decimation was an extreme punishment given to the Roman Legions when they had upset their leaders. The men would be divided into groups of 10, decide which member of their group would be executed, and carry out the execution. The survivors would then be put on a diet of barley and water for a month. These remaining 90% came away highly motivated to meet the future expectations of their leaders. (In these more enlightened times, we still carry on this tradition. We call it “layoffs.”)

This decimator is a digital finite impulse response (FIR) filter that takes the input at fS and provides a filtered output at f0. The ratio of these two frequencies is called the oversample ratio (OSR) or decimation value. The bandwidth limit in Figure 2 is for an OSR of 64. The specifics of the filter are not important for this discussion. Digital decimator filter design is a subject better suited for a future column.

Now, 9-dB/octave certainly is better than the 6 db/octave produced by the incremental ADC. An incremental ADC with a 1-Msample/s clock and 16-bit resolution has an output rate of 15 samples/s. Take the same DS modulator, and with the proper decimator, you get 16 bits of resolution at 488 samples/s. This is an improvement—not great, but definitely an improvement.

My next column will explain multiple-stage delta-sigma modulators and show how to get resolution enhancements of 15, 21, and 27 dB per octave and more.

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