Using Delta-Sigma Can Be As Easy As ADC (Part 3)

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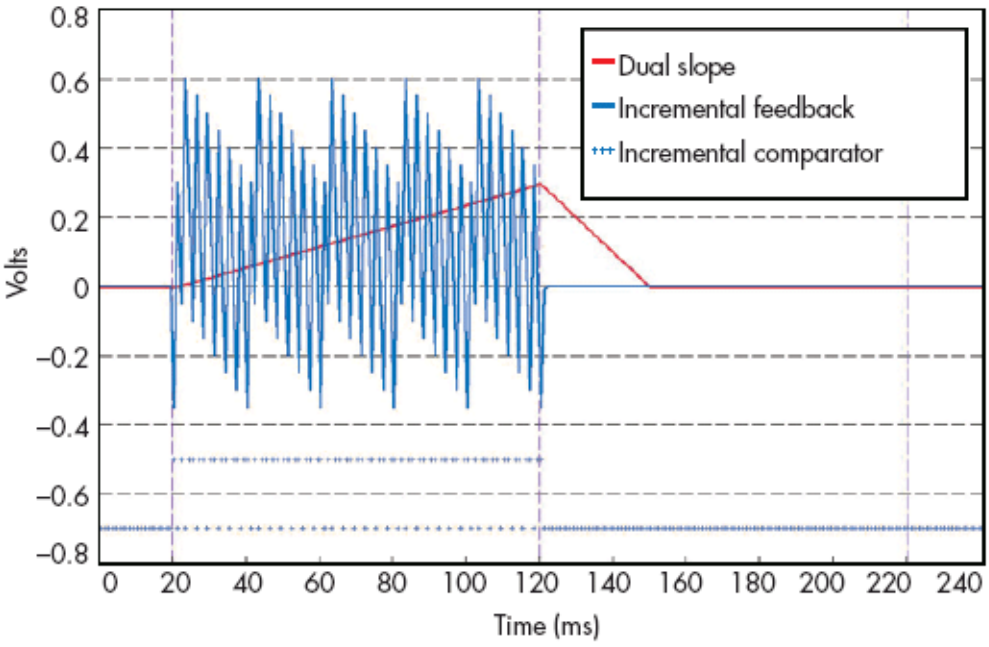
Part 2 of this series showed how a dual-slope integrator could fix the major limitations of a single slope converter.

KNOW YOUR LIMITS

Two major limitations of the dual-slope topology are comparator sensitivity and dielectric absorption. Suppose that instead of waiting until the end of the integration period to start precisely removing the charge, the references are incrementally subtracted during the integration time. Figure 1 shows a plot of this technique along with that of a dual-slope integrator. Both have an input of 0.3 V, 100-ms integration period, and references of ±1 V.



1. These waveforms for dual-slope and incremental integrators illustrate 0.3-V input, 100-count resolution.

The dual slope integrates the 0.3-V input for 100 ms and then applies the –1-V reference to start removing the acquired charge. It takes 30 ms to move the integrator output back to zero. Like the dual slope, the incremental method also integrates the input for a fixed time. Where it differs is that during the integration time, the references are constantly applied to move the output back toward zero.

For this example, the 1-V reference is subtracted 65% of the time and the –1-V reference is subtracted 35% of the time, resulting in an average of 0.3 V. The output is said to have a density of 65%. Note that the incremental method no longer requires a reintegration period.

With the charge immediately removed, there is no long-term charge to be absorbed. This eliminates the need for a poly cap. Instead, a three-cent NPO ceramic cap will suffice. For a dual slope, the integrator slope had to be set to keep the integrator in range for the whole integration period for the maximum input signal. For the incremental, with its references constantly moving the integrator back toward zero, it has to only remain within range for each clock cycle.

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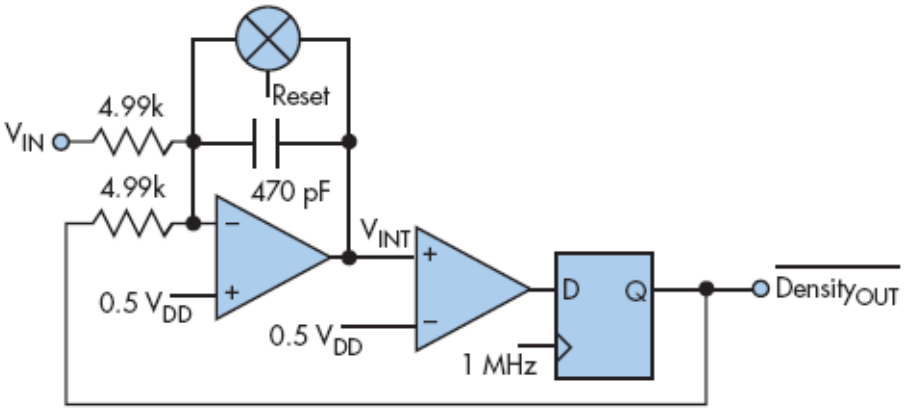
This allows for a significant increase in integrator gain, reducing the sensitivity requirement for the comparator. For a dual slope, increasing the integration time requires reducing the integrator slope. This is not the case for the incremental. The integration time can easily be increased with the integrator output guaranteed to stay in range. Figure 2 shows an incremental converter. It is called ratiometric because it uses the power supplies as references. It sounds fancier than “we didn’t provide real references.”



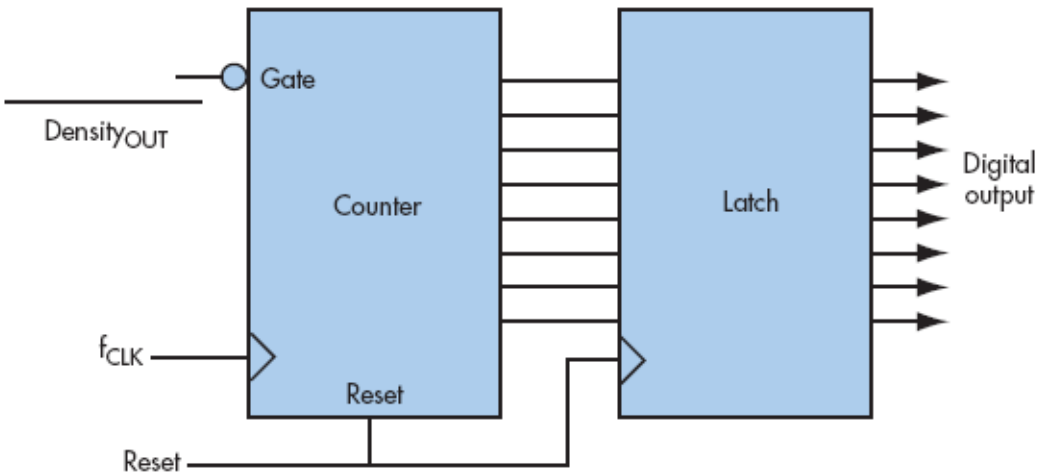
2. In this ADC, ratiometric incremental AGND = 2.5 V, V_{REF+} = +2.5 V, and V_{REF-} = –2.5 V.

The supplies are VDD and ground. The analog ground (AGND) for this system is halfway between the supplies or 0.5 VDD. For a 5-V supply and all signals referred to AGND, VREF+ is 2.5 V and VREF– is –2.5 V. The resistor and capacitor values were selected to set a slope guaranteed to stay in range for a 1-MHz sample clock.

The comparator is used to determine which reference is fed back. This negative feedback causes the output to do whatever it can to make the inputs match. So the average of the input voltages will equal the average of references:

$V_{IN} = Density_{OUT} \times V_{REF+} + (1 - Density_{OUT}) \times V_{REF-}$

All that’s needed to calculate the input voltage is to measure the density. Figure 3 shows the hardware that will do this.



3. Hardware is required to measure the incremental density.

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Setting reset causes the last value in the counter to be latched for output. The integrator is also zeroed to remove any residue from the previous sample. When reset goes low, the integrator is released, allowing the incremental converter to generate a density signal. This is used to gate the counter.

The number of clock cycles between the release and setting of reset determines the resolution. 256 cycles allows for an 8-bit value. 4096 cycles allows for a 12-bit value. With a 1-MHz clock, an 8-bit sample would have an output rate of no more than 3.9 ksamples/s while a 12-bit sample's rate would be no more than 244 samples/s.

For each doubling of the resolution, the output rate goes down by a factor of two. This is expressed as 6 db per octave or 20 db per decade. (Both 6 dB and octave are fancy ways of saying 2 while 20 db and decade are just different ways of saying 10.)

INCREMENTAL LIMITATIONS

6 dB per octave just isn't a very good resolution/sample rate tradeoff. With a 1-MHz clock, the output rate for 16-bit resolution is 15 samples/s and 1 sample/s for 20-bit resolution (multimeter-type performance). At 24 bits, it goes down to 3.5 samples per minute. If these sorts of resolutions with their corresponding sample rates are adequate for your design, an incremental converter would be a good choice. They have the advantage of design simplicity and minimal analog components. If not, different techniques need to be developed.

Here's something that's fun. I built an incremental modulator using three passive components, an op amp, a comparator, and a flip-flop. It could have been done with only the passive components and a flip-flop. Remove the op amp and build a passive RC low pass filter. Connect this filter's output to the flip-flop's input. The logic threshold hold level acts as a poor man's comparator.

Connect the inverting output of the flip-flip to the filter output. As the cap charges, its voltage increases until it exceeds the logic threshold and the flip-flop's output goes high. With the inverted input now low, the feedback resistor discharges the cap, causing it to go low. It ain't elegant, but it will win a bar bet.

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