# Using Delta-Sigma Can Be As Easy As ADC (Part 2)

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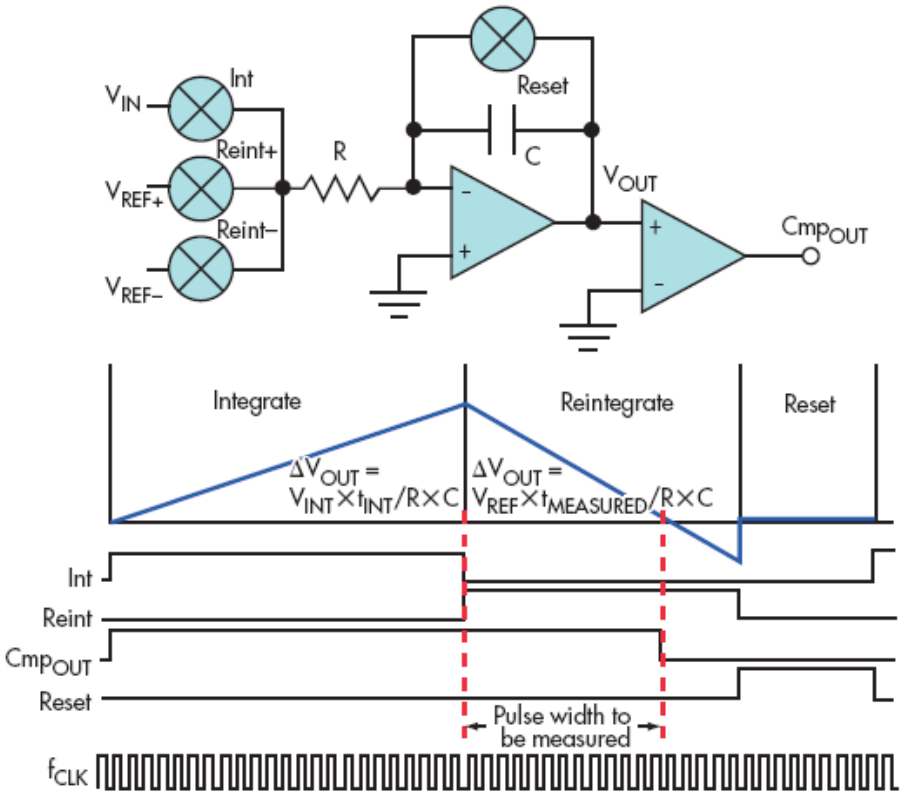
In Part 1 of the column, I took a historical approach to delta-sigma modulation with the single-slope converter.

The biggest weakness of the single-slope converter is that its accuracy depends on the component values of the integrator (ramp generator). To fix this, make sure the input voltage and reference voltage both pass through the same integrating path. The dual-slope converter shown in Figure 1 does just that.




1. With a dual-slope converter, the input and reference voltages pass through the same integrator.

Dual-slope is an integrating ADC technique that causes the digitized answer to be the average of the input signal over the integration time. This can be very useful. If the integrate time is set to one-sixtieth of a second, then any 60-Hz signals (or harmonics of 60 Hz) would be averaged to zero. This also is very useful for industrial applications where there can be a lot of mains (60-Hz power) present in signals being measured.

Of course this integration time wouldn't be of much use in Europe with its 50-Hz mains power. However, an integrate time of one-tenth of a second, or 100 ms, would remove 10 Hz and all 10-Hz harmonics, including 50, 60, 150, 180 Hz, and so on (*Fig. 2*).



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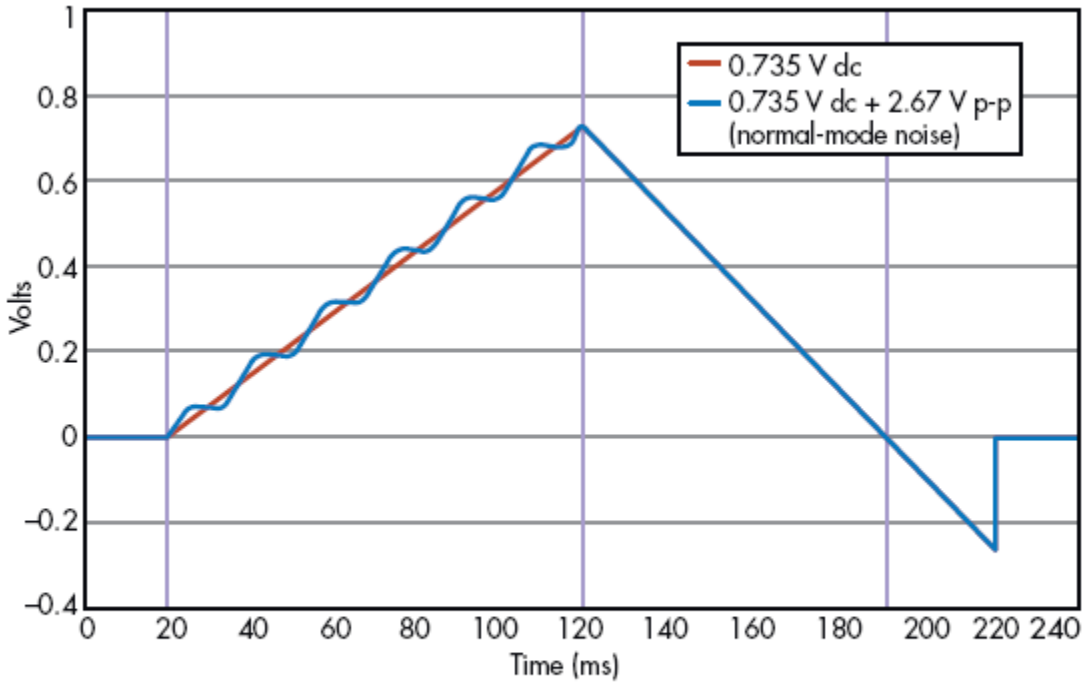



2. A dual-slope converter with a specific integration time can be used to remove mains noise.

Applying a voltage into an integrator results in the following output voltage

$$\Delta V_{OUT} = -\frac{V_{IN}}{R \times C} \times \Delta t$$

:

A dual-slope converter first integrates the input voltage for a fixed amount of time. Then, the appropriate reference ($V_{REF}$– for positive $V_{IN}$ and $V_{REF+}$ for a negative $V_{IN}$) is applied to move the integrator's output back to zero. The time it takes to completely discharge the integrator and bring the output back to zero is measured. The same amount of charge has been added and removed from the capacitor:

$$-\frac{V_{IN}}{R \times C} \times \frac{n_{INT}}{f_{CLK}} = \Delta V_{OUT} = -\frac{V_{REF}}{R \times C} \times \frac{n_{MEASURED}}{f_{CLK}}$$

Solving for $V_{IN}$:

$$V_{IN} = n_{MEASURED} \frac{V_{REF}}{n_{INT}}$$

So, you integrate an unknown signal for a fixed amount of time and integrate a known reference of opposite polarity for a measured amount to time. Because all voltages pass through the same integration path and all timing is done with the same clock, the capacitor, resistor, and clock tolerances all fall out of the equation. The input voltage is directly proportional to $n_{MEASURED}$, and $n_{INT}$ sets the resolution.

When this technique became available, single-slope converters almost immediately disappeared. Back in the late 1970s, if you were rolling your design, you most likely used CD4016 analog switches from RCA and an LM358 op amp with discrete dual JFET-differential input.

The capacitor and resistor values are selected to set the integrator slope so the integrator output stays within the power-supply rails for the maximum input voltage and integration time:

$$R \times C = \frac{V_{INMAX}}{V_{OUTMAX}} \times \frac{n_{INTMAX}}{f_{CLK}}$$

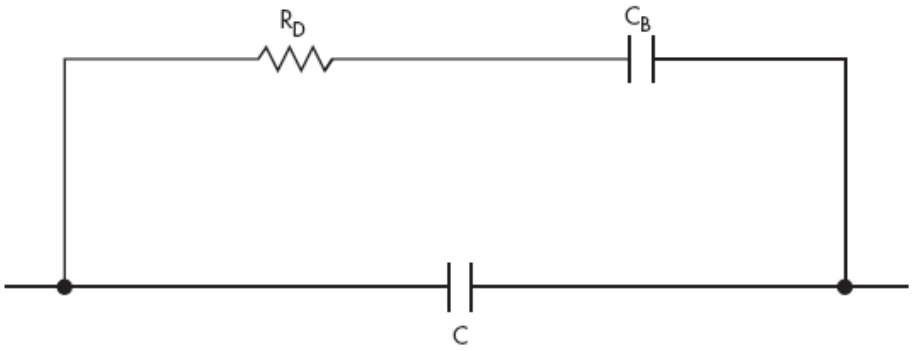
If you wanted an integrated solution, most likely you used a 7106 panel meter chip from Intersil.

## *DUAL-SLOPE LIMITATIONS*

A dual-slope ADC has several limitations. Increasing the resolution requires the integration time or sample clock to be increased. To keep the output within its power-supply rails, a longer integrate time requires a proportional reduction in the integrator's slope.

Each bit of resolution is now proportionally less voltage, taxing the comparator's sensitivity. Comparator sensitivity is a function of cost. However, increasing the clock frequency taxes the comparator's response time. Comparator response time is also a function of cost.

The last and most likely most significant limitation is dielectric absorption, or soakage, of the integrating capacitor. Electrons stored in a capacitor tend to be absorbed. Figure 3 shows the equivalent electrical model of this effect. This means that not all the charge placed on the capacitor during integration time can be removed.




3. Dielectric absorption has a significant effect on the capacitor.

One solution is to use a capacitor with the lowest possible dielectric absorption. Commercially, that would be the "poly" caps—polycarbonate, polyester, polypropylene, polystyrene. These capacitors are readily available but expensive, typically about a dollar each.

Still, the dual slope has many advantages. This easy-to-construct topology can function with 20 to 24 bits of resolution. If you're okay with paying a dollar for a capacitor, this may be the ADC for you. It's still available commercially.

Part 3 will show how some simple variations in how the reintegration is done impact comparator sensitivity, as well as how response time can be reduced and how the need for a hyper-low dielectric absorption cap can be eliminated.

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