Cypress Semiconductor
Technology Qualification Report

S050001 VERSION 1.0
June 2005

TSMC Fab 3, 0.35um	
ASIC	**SMaL Camera ASIC**

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

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PRODUCT QUALIFICATION HISTORY

Qual Report	Description of Qualification Purpose	Date Comp
S050001	New Technology, TSMC Fab 3, 0.35um ASIC	Dec 03

PRODUCT DESCRIPTION (for qualification)		
Qualification Purpose: Qualify New Technology, TSMC 0.35um, ASIC		
Marketing Part #:		
Device Description:		
Cypress Division:	Cypress Semiconductor Corporation – Memory and Imaging Division (MID)	
Overall Die (or Mask) REV Level (pre-requisite for qualification):		
Die Size (stepping):	4195 x 4195 um2	

SMaLCamera Part #	Product Information	TSMC Part #
ASIC		TMK212B

TECHNOLOGY/FAB PROCESS DESCRIPTION			
Number of Metal Layers:	5	Metal Composition:	
Passivation Type and Materials:			
Free Phosphorus contents in top glass layer(%):			
Generic Process Technology/Design Rule (μ-drawn):			
Gate Oxide Material/Thickness (MOS):			
Name/Location of Die Fab (prime) Facility:	TSMC		
Die Fab Line ID/Wafer Process ID:	Fab 3		

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY SITE FACILITY
144L TFBGA	**SPIL, Taiwan**

Note: Package Qualification details upon request.

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MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	TFBGA
Package Outline, Type, or Name:	10 x 10
Mold Compound Name/Manufacturer:	SMT-B-1N
Mold Compound Flammability Rating:	
Oxygen Rating Index:	
Substrate Designation:	
Substrate Material / Supplier	Ryowa 4 layer substrate
Ball, Composition / Diameter:	63% Sn / 37% Pb, 0.6mm
Die Backside Preparation Method/Metallization:	
Die Separation Method:	
Die Attach Supplier:	Ablebond
Die Attach Material:	8355F
Bond Diagram Designation	
Wire Bond Method:	
Wire Material/Size:	Au / 1.0mil
Thermal Resistance Theta JA °C/W:	
Package Cross Section Yes/No:	
Assembly Process Flow:	
Name/Location of Assembly (prime) facility:	SPIL, Taiwan

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	SPIL, Taiwan
Fault Coverage:	100%

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[3]	Failure Rate
High Temperature Operating Life Early Failure Rate	0	0	N/A	N/A	N/A
High Temperature Operating Life[1,2,] Long Term Failure Rate	100,000, DHRs	0	0.7	55	55 FIT

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate.
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

QUALIFICATION TEST RESULTS

Test	Standard	Condition	Read Points	Results	Pass / Fail
ESD-HBM	JESD22-A114-B		500V 2000	0/3 3/3	Pass
ESD-MM	JESD22-A115-A		100V 200	0/3 3/3	Pass
High Temp Storage		175C	500hr 1000	0/231 0/231	Pass
High Temp Operating Life (LFR)	883D M1015.8	125C, 3.6V, 1MHz	168hr 500 1000	0/300 0/300 0/300	Pass
Latch Up	JESD78	25C	Itest	0/5	Pass
Pressure Cooker		121C, 100% RH, 2ATM	168hr	0/77	Pass
Pressure Cooker		133C, 100% RH 2ATM	168hr	0/231	Pass
Temp Cycle		MSL3 Precon Cond C	1000cy	0/77	Pass
Temp Cycle	883D M1010.7	Cond C	500cy 1000	0/231 0/229	Pass
Temp-Humidity-Bias		85C/85%RH, 3.3V	168hr 500 1000	0/231 0/231 0/231	Pass
Thermal Shock		MSL3 Precon Cond C	500cy	0/77	Pass
Thermal Shock	883D M1011.9	Cond C	200cy 500	2/231 7/229	Fail (*)

(*) Attributed to assembly problem. See TSMC spec T-035-LO-QR-001