Cypress Semiconductor
Product Qualification Report

QTP# L000004 VERSION 1.0
October, 2001

CYNCP80192-BGC Network Co-Processor
TSMC 0.25um Technology, Fab 5 (TSMC)

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

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PRODUCT QUALIFICATION HISTORY

Qual Report	Description of Qualification Purpose	Date Comp
G990001	New Technology TSMC 0.25um 4T 3P2M /New Product, 8Meg, GVT71256B36 and its product family and bonding / metal option	Oct 99
L000004	New Network Co-Processor, CYNCP80192-BGC	Oct 01

PRODUCT DESCRIPTION (for qualification)			
Qualification Purpose: Qualify New Device CYNCP80192-BGC			
Marketing Part #:	Cypress Part# = CYNCP80192-BGC (Lara Device# LNI8010)		
Device Description:	Network Co-Processor		
Cypress Division:	Cypress Semiconductor Corporation – Data Communication Division (DCD)		
Overall Die (or Mask) REV Level (pre-requisite for qualification):		Rev. A	
Die Size (stepping):	229 mils X 229 mils	What ID markings on Die:	LNT2501COP

TECHNOLOGY/FAB PROCESS DESCRIPTION			
Number of Metal Layers:	4	Metal Composition:	Al - 0.5%Cu
Passivation Type and Materials:	Oxide / Nitride		
Free Phosphorus contents in top glass layer(%):	0%		
Number of Transistors in Device:	1,233,478		
Number of Gates in Device:	26,190		
Generic Process Technology/Design Rule (µ-drawn):	COMS, T025LV		
Gate Oxide Material/Thickness (MOS):	SiO_2 / 50Å		
Name/Location of Die Fab (prime) Facility:	TSMC Taiwan		
Die Fab Line ID/Wafer Process ID:	Fab5, CMOS, 0.25 microns, Low Voltage, 4Metal, 1Poly, (TSMC)		

PACKAGE AVAILABILITY

PACKAGE	**ASSEMBLY FACILITY SITE**
388 BGA	**ASE TAIWAN**

Note: Package Qualification details upon request

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	Not Applicable
Package Outline, Type, or Name:	388 BGA
Mold Compound Name/Manufacturer:	KE-1100A / Toshiba
Mold Compound Flammability Rating:	V-0 per UL94
Oxygen Rating Index:	> 28%
Substrate Material:	BT Resin
Lead Finish, Composition / Thickness:	Solder Ball, 63%Sn, 37%Pb
Die Backside Preparation Method/Metallization:	N/A
Die Separation Method:	Wafer Saw
Die Attach Supplier:	Ablestik
Die Attach Material:	Epoxy
Bond Diagram Designation	K-B-ASE-0272B8A-01 Rev.A
Wire Bond Method:	Thermosonic
Wire Material/Size:	99.99% gold / 1.1 mil dia
Thermal Resistance Theta JA °C/W:	26.8°C/W
Package Cross Section Yes/No:	N/A
Assembly Process Flow:	ASE SPEC# 64-04-000-0348
Name/Location of Assembly (prime) facility:	ASE Taiwan

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	ASE Taiwan
Fault Coverage:	100%

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc Max= 2.75V, 125°C	P
High Accelerated Saturation Test (HAST)	130°C, 2.75V,85%RH Precondition: JESD22 Moisture Sensitivity Level 3 192 Hrs., 30°c/60% RH + 3IR Reflow, 220°C	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition ?, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity Level 3 192 Hrs., 30°c/60% RH + 3IR Reflow, 220°C	P
Pressure Cooker Test	No bias, 130°C, 85%RH	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,000V MIL-STD-883, Method 3015.7	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V	P
Static Latchup Sensitivity	100°C, ± 200mA	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[3]	Failure Rate[4]
High Temperature Operating Life Early Failure Rate	N/A	N/A	N/A	N/A	N/A
High Temperature Operating Life[1,2] Long Term Failure Rate	116,000 DHRs	0	0.7	N/A	143 FIT

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate.
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A = The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

[4] **Technology Qualification FIT Rate = 48, QTP #G990001**

Reliability Test Data

QTP #: L000004

High Temperature Operating Life (HTOL)

Test	Lot No	Temp. Cycle	Voltage	SS	Duration	Result Pass/Rej
HTOL	COP000001	125C	2.75V	116	1000hrs	100/0

Temperature Cycle (TC)

Test	Lot No	Temp C	Duration	SS	Result Pass/Rej
T/C	COP000001	-65° to 150°C	1000 Cycles	45hrs	45/0

High Acceleration Stress Test (HAST)

Test	Lot No	Temp. C	Voltage	Relative Humidity (85%)	SS	Duration	Result Pass/Rej
HAST	COP000001	130°C	2.75V	85%RH	45	100hrs	45/0

Pressure Cooker Test

Test	Lot No	Temp. C	Relative Humidity (85%)	SS	Duration	Result Pass/Rej
PCT	COP000001	130°C	85%RH	45	168hrs	45/0

High Temperature Storage

Test	Lot No	Temp. C	SS	Duration	Result Pass/Rej
HTS	COP000001	150°C	77	1000hrs	77/0

Thermal Shock

Test	Lot No	Temp. C	SS	Duration	Result Pass/Rej
TS	COP000001	-65°C to 150°C	45	200 Cycles	45/0

Reliability Test Data

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Human Body Model (HBM)

Test	Lot No	Bias	SS	Duration	Result Pass?Rej
HBM MIL-STD-883, Method 3015.7	COP000001	> 2,000 Volts	6	COMP	6/0

Charge Device Model (CDM)

Test	Lot No	Bias	Sample Size	Duration	Result Pass/Rej
CDM	COP000001	500V	2	COMP	2/0

Latch-up

Test	Lot No	Temp. Cycle	Bias	Sample Size	Duration	Result Pass/Rej
Latch-up	COP000001	25°C to 100°C	> ± 200mA	4	COMP	4/0

Note: Qualification was done per Lara standard before Cypress Semiconductor acquisition.