Cypress Semiconductor
Technology Qualification Report

G990003 VERSION 1.0
May, 2001

WaferTech 0.35um	
GVT71128B36Y / GVT71128E36Y	**128 x 36**
GVT71128G36Y	**128 x 36**
GVT71256B18Y / GVT71256D18Y	**256 x 18**
GVT71256E18Y / GVT71256F18Y	**256 x 18**
GVT71256G18Y	**256 x 18**

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

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PRODUCT QUALIFICATION HISTORY

Qual Report	Description of Qualification Purpose	Date Comp
G990003	New Technology, WaferTech 0.35um / 4Meg, Asynchronous RAM, GVT71128E36, its product family and bonding option	Jan 98

PRODUCT DESCRIPTION (for qualification)		
Qualification Purpose: Qualify New Technology, WaferTech 0.35um, 4Meg, Asynchronous RAM, GVT71128E36, its product family and its bonding option		
Marketing Part #:	GVT71128E36	
Device Description:	3.3V, Commercial available in 100-pin TQFP package.	
Cypress Division:	Cypress Semiconductor Corporation – Memory Product Division (MPD)	
Overall Die (or Mask) REV Level (pre-requisite for qualification):		Rev. Y
What ID markings on Die:	GVT71128E36	

Galvantech Part #	Product Information	TSMC Part #
GVT71128B36Y		TM6783
GVT71128E36Y		TM6783
GVT71128G36Y	B,C,D: 3.3V	TM6783
GVT71256B18Y	E, F, G: 2.5V	TM6783
GVT71256D18Y	128E36 and 128G36 are bonding option	TM6783
GVT71256E18Y	256B18 and 256D18 are bonding option	TM6783
GVT71256F18Y	256E18, 256F18, and 256G18 are bonding option	TM6783
GVT71256G18Y		TM6783

TECHNOLOGY/FAB PROCESS DESCRIPTION			
Number of Metal Layers:	2	Metal Composition:	Metal 1: 4,000K Å Ti/1,000K Å TiN/4,000K Å AlCu/250K Å TiN Metal 2: 1,500K Å Ti/6,000K Å AlCu/250K Å TiN
Passivation Type and Materials:			2K PE-Oxide + 6.5K PE-Nitride
Free Phosphorus contents in top glass layer(%):			0
Generic Process Technology/Design Rule (µ-drawn):			CMOS, Double Metal, 0.35um
Gate Oxide Material/Thickness (MOS):			70A SiO2
Name/Location of Die Fab (prime) Facility:			WaferTech, WA, USA
Die Fab Line ID/Wafer Process ID:			WaferTech 0.35um

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY SITE FACILITY
100-pin TQFP	**SPIL/ ASEK**

Note: Package Qualification details upon request.

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MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	A100
Package Outline, Type, or Name:	100-pin Thin Quad Flat Package (TQFP)
Mold Compound Name/Manufacturer:	Hitachi 7320
Mold Compound Flammability Rating:	V-O per UL94
Oxygen Rating Index:	>28%
Lead Frame Material:	Copper
Lead Finish, Composition / Thickness:	85%Sn, 15%Pb
Die Backside Preparation Method/Metallization:	N/A
Die Separation Method:	Wafer Saw
Die Attach Supplier:	Ablestik
Die Attach Material:	Ablestik 8361H
Bond Diagram Designation	GV-D100-9051801
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au, 1.0um
Thermal Resistance Theta JA °C/W:	29.9 °C/W
Package Cross Section Yes/No:	N/A
Assembly Process Flow:	49-78002
Name/Location of Assembly (prime) facility:	SPIL/ASEK

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	CHIPMOS
Fault Coverage:	100%

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENTS

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc = 3.6V, 150°C (500hrs)	R
High Accelerated Saturation Test (HAST	130C, 85%RH,	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C	P
Pressure Cooker Test	100%RH, 15PSIG	P
High Temperature Storage (Plastic)	150C	P
Electrostatic Discharge Human Body Model (ESD-HBM)	MIL-STD-883C (2000V)	P
Thermal Shock	-65°C to 150°C	P
Latchup Sensitivity	In Accordance with JEDEC 17. 9V, +/-300mA	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[3]	Failure Rate
High Temperature Operating Life Early Failure Rate	4280	0	N/A	N/A	0 PPM
High Temperature Operating Life[1,2,] Long Term Failure Rate	1,881,812, DHRs	0	0.7	170	6 FIT

[1]ssuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2]Chi-squared 60% estimations used to calculate the failure rate.
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

HTOL Reliability Monitor					
Dynamic BI @ 150C, Vcc=3.63V					
Read hr	0	24	184	368	500
SS	1960	-	1960	1959	725
Rej	0	0	0	0	1
SS	1885	1885	1885	1885	1885
Rej	0	0	0	0	0

HTOL Qualification					
Read hr	0	24	184	368	500
SS	435	435	435	-	435
Rej	0	0	0	-	0

Wafer Level

Electromigration (EM)

Pattern	Fail Criteria >20% Change	Jmax>Jtsmc @ 0.1% CUM failure, 100k hoursn @ 110C, sample size 30 units. (Units in mA/um)					
		C92050		C92051		C92054	
M1 (0.4um)	1.0mA/um	>1.9	Pass	>3.74	Pass	>3.71	Pass
M1 (7um)	1.0mA/um	2.36	Pass	>1.59	Pass	>1.48	Pass
M2 (0.45um)	1.2mA/um	>5.61	Pass	>5.56	Pass	>5.46	Pass
M2 (7um)	1.2mA/um	2.32	Pass	2.16	Pass	2.07	Pass
Via (0.4 x 0.4)	0.34mA/um	>0.94	Pass	>0.94	Pass	>0.93	Pass
Via (0.45 x .45)	0.3mA/um	>1.04	Pass	>1.06	Pass	>1.05	Pass
Co (0.4 x 0.4)	0.41mA/um	>0.64	Pass	>0.64	Pass	>0.63	Pass

*Stress Conditions: 175°C

Hot Carrier (HEI)

Lot #	Gate	Fail Criteria= .1% CUM @ Vcc+10%> 0.2yr	Reading (year)	Results*
C92050	20/0.3um	Idsat Shift >10%	0.52	Pass
C92051	20/0.3um	Idsat Shift >10%	0.46	Pass
C92054	20/0.3um	Idsat Shift >10%	0.68	Pass

Test Condition: 10 pieces, Vds=4.5V for 12k minutes @ 25C.

Gate Oxide Integrity (GOI)

Pattern		C92050	C92051	C92054
(A)	Mode A Fail (%)	0	0	0
N-Well: 180,00um^2;	Mode B Fail (%)	0.34	0	0
Tox=70Å	Yield	99.66	100	100
(B)	Mode A Fail (%)	0	0	0
P-Well: 180,00um^2;	Mode B Fail (%)	0.34	0	0
Tox=70Å	Yield	99.66	100	100

Mode A: Vbd <=3.3V
Mode B: 3.3VVbd <8V