Cypress Semiconductor
Product Qualification Report

G000001 VERSION 1.0
May, 2001

8Meg Synchronous SRAM TSMC 0.25um	
GVT71256ZB36Z / GVT71256ZC36Z	**256 x 36**
GVT75256ZC36Z	**256 x 36**
GVT71512ZB18Z / GVT71512ZC18Z	**512 x 18**
GVT75512ZC18Z	**512 x 18**

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

Ed Russell
Reliability Director
(408) 432–7069

Kim-Ngan Nguyen
Staff Reliability Engineer
(408) 943–2136

PRODUCT QUALIFICATION HISTORY

Qual Report	Description of Qualification Purpose	Date Comp
G990001	New Technology, TSMC 0.25um / 8Meg, Synchronous SRAM, GVT71256B3, and product family, bonding and metal option	Oct 99
G000001	New Product, 8Meg, Synchronous SRAM, GVT71256ZC36Z, and product family, bonding and metal option, TSMC 0.25um	Sep 00

PRODUCT DESCRIPTION (for qualification)		
Qualification Purpose: New 8Meg, Synchronous SRAM, GVT71256ZC36Z and product family, bonding and metal option, TSMC 0.25um		
Marketing Part #:	GVT71256ZC36Z	
Device Description:	2.5V, Commercial/Industrial available in 100-pin TQFP package.	
Cypress Division:	Cypress Semiconductor Corporation – Memory Product Division (MPD)	
Overall Die (or Mask) REV Level (pre-requisite for qualification):		Rev. Z
What ID markings on Die:	GVT71256ZC36	

Galvantech Part #	Product Information	TSMC Part #
GVT71256ZB36Z		TM7853
GVT71256ZC36Z		TM7853
GVT75256ZC36Z		TM7853
GVT71512ZB18Z		TM7853
GVT71512ZC18Z		TM7853
GVT75512ZC18Z		TM7853

TECHNOLOGY/FAB PROCESS DESCRIPTION			
Number of Metal Layers:	2	Metal Composition:	Metal 1: 4,000Å Al Cu/7,000Å TiN Metal 2: 1,000Å Tin/6,000Å AlCu/250Å TiN
Passivation Type and Materials:		1,500Å SiON, 5,000Å SOG, 10,000PESONÅ	
Free Phosphorus contents in top glass layer(%):		0	
Generic Process Technology/Design Rule (□-drawn):		CMOS, Double Metal, 0.25um,	
Gate Oxide Material/Thickness (MOS):		70A, SiO2	
Name/Location of Die Fab (prime) Facility:		TSMC, Taiwan Roc.	
Die Fab Line ID/Wafer Process ID:		TSMC 0.25um	

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY SITE FACILITY
100-pin TQFP	**SPIL/ ASEK**

Note: Package Qualification details upon request.

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	A100
Package Outline, Type, or Name:	100-pin Thin Quad Flat Package (TQFP)
Mold Compound Name/Manufacturer:	Hitachi 7320
Mold Compound Flammability Rating:	V-O per UL94
Oxygen Rating Index:	>28%
Lead Frame Material:	Copper
Lead Finish, Composition / Thickness:	85%Sn, 15%Pb
Die Backside Preparation Method/Metallization:	N/A
Die Separation Method:	Wafer Saw
Die Attach Supplier:	Sumitomo
Die Attach Material:	Sumitomo 7320
Bond Diagram Designation	ABSR-00134
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au, 1.0um
Thermal Resistance Theta JA °C/W:	29.9 °C/W
Package Cross Section Yes/No:	N/A
Assembly Process Flow:	49-78002
Name/Location of Assembly (prime) facility:	SPIL/ASEK

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	CHIPMOS
Fault Coverage:	100%

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc Max=3.6V, 150°C	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc Max=3.6V, 150°C	P
High Accelerated Saturation Test (HAST)	130°C, ,85%RH	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C	P
Electrostatic Discharge Human Body Model (ESD-HBM)	MIL-STD-883, Method 3015.7 (2,000V)	P
Latchup Sensitivity	In accordance with JEDEC 17. Cypress Spec. 01-00081, 5.4V, <500mA	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[3]	Failure Rate[4]
High Temperature Operating Life Early Failure Rate	304	0	N/A	N/A	0 PPM
High Temperature Operating Life[1,2,] Long Term Failure Rate	152,000 DHRs	0	0.7	170	35 FIT

[1]ssuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2]Chi-squared 60% estimations used to calculate the failure rate.
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

[4] EFR and LFR Failure Rate based on TSMC 0.25um 4T 3P2M Technology.

Precondition - JESD-A113-B

TSMC .25um 8megS GVT71256ZC36I			Condition: Level 3, 192 Hrs @ 30°C/60% RH			
Device	Lot Number	Package	In	Out	Rej	Yield
GVT71256ZC36	C623224BB1	100TQFP	77	77	77	100.0%

HTOL - MIL-STD-883, Method 3015

TSMC .25um 4megS GVT71256ZC36			Condition: Dynamic BI @ 150C, Vcc=3.6V, Vih =3V					Reliabilty	
Device	Lot Number	Package	Read(hr)	0	24	184	500	TDH	
GVT71256ZC36	C62324BB1	100TQFP	SS/Rej	77	77	77	77	38,500	
					0	0	0	-	

ESD - MIL-STD-883, Method 3015

TSMC .25um 8megS GVT71256ZC36			Condition: Human Body Model						
Device	Lot Number	Package	Stress	1kV	1.5kV	2kV	2.5kV	3kV	3.5kV
GVT71256ZC36	C62324BB1	100TQFP	SS/Rej			3			
						0			

A blank entry indicates ESD stress was not performed for that level.

ESD Rating:

Device	Voltage
GVT71256ZC36	2kV

IC Latch-up - JESD78

TSMC .25um 8megS 71256ZC36			Stress Condtions				Vcc		Input/IO	
Device	Lot Number	Package	Read	Condition	Results	Forcing	IN = HI	IN = LO	Pos (Hi/Lo)	Neg (Hi/Lo)
GVT71128CA36	C62324BB1	100TQFP	SS/Rej	Class II	6	Voltage	5.4V	5.4V	5.4V	-1.8V
				(125C)	0	Current	< 500mA	< 500mA	128mA	-100ma

Triple Poly Double Metal SRAM Process in 100TQFP

Precondition - JESD-A113-B

TSMC .25um/ GVT 8 MegS Qual			Condition: Level 3, 192 Hrs @ 30°C/60% RH			
Device	Lot Number	Package	In	Out	Rej	Yield
GVT71256B36T	C617730B5ADE5	100TQFP	77	77	0	100.0%
GVT71256B36T	C61905B1ADE1	100TQFP	77	77	0	100.0%
GVT71256B36T	C61960DA	100TQFP	73	73	0	100.0%

Temperature Cycle - JESD22-A104A

TSMC .25um/ GVT 8 MegS Qual			Condition: -65°C/150°C, 1000 Cycles		
Device	Lot Number	Package	Read	0 Cycle	1000 Cycles
GVT71256B36T	C619050B1ADE1	100TQFP	SS/Rej	77 0	77 0
GVT71256B36T	C61960DA	100TQFP	SS/Rej	77 0	77 0
GVT71256B36T	C62172GA	100TQFP	SS/Rej	77 0	77 0

HAST - JESD22-A110-B

TSMC .25um/ GVT 8 MegS Qual			Condition: 100 Hrs @ 130°C/85% RH		
Device	Lot Number	Package	Read	0 Hour	100 Hours
GVT71256B36T	C619050B1ADE1	100TQFP	SS/Rej	45 0	45 0
GVT71256B36T	C61960DA	100TQFP	SS/Rej	45 0	45 0
GVT71256B36T	C62172GA	100TQFP	SS/Rej	45 0	45 0

HTOL - MIL-STD-883, Method 3015

TSMC .25um/ GVT 8 MegS Qual			Condition: Dynamic BI @ 150C, Vcc=3.6V, Vih =3V					Reliabilty
Device	Lot Number	Package	Read(hr)	0	24	184	500	TDH
GVT71256B36T	C617730B5ADE5	100TQFP	SS/Rej	77 0	77 0	77 0	77 0	38,500 -
GVT71256B36T	C619050B1ADE1	100TQFP	SS/Rej	77 0	77 0	77 0	77 0	38,500 -
GVT71256B36T	C61960DA	100TQFP	SS/Rej	73 0	73 0	73 0	73 0	36,500 -
							Total SS/Rej	**113,500 -**

ESD - MIL-STD-883, Method 3015

TSMC .25um/ GVT 8 MegS Qual			Condition: Human Body Model						
Device	Lot Number	Package	Stress	1kV	1.5kV	2kV	2.5kV	3kV	3.5kV
GVT71256B36T	C617730B5ADE5	100TQFP	SS/Rej			3 0			
GVT71256B36T	C619050B1ADE1	100TQFP	SS/Rej			3 0			
GVT71256B36T	C61960DA	100TQFP	SS/Rej			3 0			

A blank entry indicates ESD stress was not performed for that level.

IC Latch-up - JESD78

TSMC .25um/ GVT 8 MegS Qual			Stress Condtions				Vcc		Input/IO	
Device	Lot Number	Package	Read	Condition	Results	Forcing	IN = HI	IN = LO	Pos (Hi/Lo)	Neg (Hi/Lo)
GVT71256B36T	C617730B5ADE5	100TQFP	SS/Rej	Class I (25C)	6 0	Voltage Current	5.4V < 500mA	5.4V < 500mA	5.4V 124mA	-1.8V -100ma
GVT71256B36T	C619050B1ADE1	100TQFP	SS/Rej	Class II (125C)	6 0	Voltage Current	5.4V < 500mA	5.4V < 500mA	5.4V 124mA	-1.8V -100ma
GVT71256B36T	C61960DA	100TQFP	SS/Rej	Class II (125C)	6 0	Voltage Current	5.4V < 500mA	5.4V < 500mA	5.4V 124mA	-1.8V -100ma
GVT71256B36T	C62172GA	100TQFP	SS/Rej	Class II (125C)	6 0	Voltage Current	5.4V < 500mA	5.4V < 500mA	5.4V 124mA	-1.8V -100ma

Electromigration (EM)

Pattern	Fail Criteria >20% Change	Jmax>Jtsmc @ 0.1% CUM failure, 100k hoursn @ 110C, sample size 30 units. (Units in mA/um)					
		C92050		C92051		C92054	
M1 (0.4um)	1.0mA/um	>1.9	Pass	>3.74	Pass	>3.71	Pass
M1 (7um)	1.0mA/um	2.36	Pass	>1.59	Pass	>1.48	Pass
M2 (0.45um)	1.2mA/um	>5.61	Pass	>5.56	Pass	>5.46	Pass
M2 (7um)	1.2mA/um	2.32	Pass	2.16	Pass	2.07	Pass
Via (0.4 x 0.4)	0.34mA/um	>0.94	Pass	>0.94	Pass	>0.93	Pass
Via (0.45 x .45)	0.3mA/um	>1.04	Pass	>1.06	Pass	>1.05	Pass
Co (0.4 x 0.4)	0.41mA/um	>0.64	Pass	>0.64	Pass	>0.63	Pass

*Stress Conditions: 175^{o}C

Hot Carrier (HEI)

Lot #	Gate	Fail Criteria= .1% CUM @ Vcc+10%> 0.2yr	Reading (year)	Results*
C92050	20/0.3um	Idsat Shift >10%	0.52	Pass
C92051	20/0.3um	Idsat Shift >10%	0.46	Pass
C92054	20/0.3um	Idsat Shift >10%	0.68	Pass

Test Condition: 10 pieces, Vds=4.5V for 12k minutes @ 25C.

Gate Oxide Integrity (GOI)

Pattern		C92050	C92051	C92054
(A) N-Well: 180,00um^{2}; Tox=70Å	Mode A Fail (%) Mode B Fail (%) Yield	0 0.34 99.66	0 0 100	0 0 100
(B) P-Well: 180,00um^{2}; Tox=70Å	Mode A Fail (%) Mode B Fail (%) Yield	0 0.34 99.66	0 0 100	0 0 100

Mode A: Vbd <=3.3V
Mode B: 3.3VVbd <8V