Cypress Semiconductor
Technology Derivative Qualification Report

QTP# 99396 VERSION 2.0
November 2005

R52LD-5R, Fab 4	
CY62128B	**1-Mbit (128K x 8) Static RAM**

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

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PRODUCT QUALIFICATION HISTORY

Qual Report	Description of Qualification Purpose	Date Comp
99396	New Technology Derivative R52LD-5R /New 1Meg, SRAM, CY62128B	Sep 00

PRODUCT DESCRIPTION (for qualification)		
Qualification Purpose: To qualify New Technology Derivative R52LD-5R, Fab 4 and 1Meg SRAM, CY62128B.		
Marketing Part #:	CY62128B	
Device Description:	4.5V-5.5V, Commercial and Industrial available in 32-Lead SOIC/TSOP	
Cypress Division:	Cypress Semiconductor Corporation – Memory Product Division (MPD)	
Overall Die (or Mask) REV:		Rev. H
What ID markings on Die:	7C62128/7C1128	

TECHNOLOGY/FAB PROCESS DESCRIPTION - R52LD-5R			
Number of Metal Layers:	2	Metal Composition:	Metal 1: 500 Å TiW/6000 Å Al-.5%Cu/300 Å TiW Metal 2: 300Å CoTi /8000Å Al-.5%Cu/300Å TiW
Passivation Type and Materials:	1000Å PECVD Oxide, 9000Å PECVD Si_3N_4		
Free Phosphorus contents in top glass layer (%):	0%		
Generic Process Technology/Design Rule (μ-drawn):	CMOS, Double Metal, 0.25 μm/0.3 FETS		
Gate Oxide Material/Thickness (MOS):	70Å (core) 110Å Regulator		
Name/Location of Die Fab (prime) Facility:	Cypress Semiconductor - Bloomington, MN		
Die Fab Line ID/Wafer Process ID:	Fab4/R52LD-5R		

PACKAGE AVAILABILITY

PACKAGE TYPE	ASSEMBLY SITE FACILITY
32-Lead TSOP	**TAIWN-T**
32-Lead SOIC	**CSPI-R**

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATIPON	
Package Designation:	S32
Package Outline, Type, or Name:	32-Lead Plastic Small Outline Ics (SOIC)
Mold Compound Name/Manufacturer:	Nitto MP8000CH4-A2
Mold Compound Flammability Rating:	V-O per UL94
Oxygen Rating Index:	>28%
Lead Frame Material:	Copper
Lead Finish, Composition / Thickness:	Solder Plated 85%Sn, 15%Pb
Die Backside Preparation Method/Metallization:	N/A
Die Separation Method:	Wafer Saw
Die Attach Supplier:	Ablestik
Die Attach Material:	8361H
Bond Diagram Designation	10-03682
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au, 1.0mil
Thermal Resistance Theta JA °C/W:	48.8°C/W
Package Cross Section Yes/No:	N/A
Assembly Process Flow:	11-21000
Name/Location of Assembly (prime) facility:	Cypress Philippines (CSPI-R)

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	Cypress Philippines (CSPI-R)
Fault Coverage:	100%

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc = 5.75V, 150°C	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc = 5.75V, 150°C	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65C to 150C Precondition: JESD22 Moisture Sensitivity MSL 3 192 hrs, 30C/60%RH+3IR-Reflow, 220°C+0, -5°C	P
Pressure Cooker	121C, 100%RH Precondition: JESD22 Moisture Sensitivity MSL 3 192 hrs, 30C/60%RH+3IR-Reflow, 220°C+0, -5°C	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V MIL-STD-883, Method 3015.7	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V Cypress Spec. 25-00020	P
Static Latch-up	125C, 11.5V, ± 300mA In accordance with JEDEC 17. Cypress Spec. 01-00081	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Acceleration Factor[4]	Failure Rate
High Temperature Operating Life Early Failure Rate[1]	2,802 Devices	0	N/A	N/A	0 PPM
High Temperature Operating Life[2, 3] Long Term Failure Rate	201,728 HRs	0	0.7	170	27 Fit

[1] A production burn-in of 12 Hrs at 150°C, 6.8V is required for the product.
[2] Assuming an ambient temperature of 150°C and a junction temperature rise of 15°C.
[3] Chi-squared 60% estimations used to calculate the failure rate.
[4] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

Reliability Test Data

QTP #: 99396

Device	*Fab Lot #*	*Assy Lot #*	*Assy Loc*	*Duration*	*Samp*	*Rej*	*Failure Mechanism*
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (150C, 5. 75V, >Vcc Max)							
CY62128B-ZAC	4020039	*610027419*	CSPI-R	48	2802	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (150C, 5. 75V, >Vcc Max)							
CY62128B-ZAC	4020039	*610028034*	CSPI-R	512	394	0	
STRESS: ESD-CHARGE DEVICE MODEL (500V)							
CY62128B-SC	4020039	*610028034*	CSPI-R	COMP	9	0	
ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015 (2,200V)							
CY62128B-SC	4020039	*610028034*	CSPI-R	COMP	9	0	
STRESS: STATIC LATCH-UP TESTING (125C, 11.5V, +/-300mA)							
CY62128B-SC	4020039	*610028034*	CSPI-R	COMP	3	0	
STRESS: PRESSURE COOKER TEST (121C, 100%RH), PRE COND 192HRS 30C/60%RH (MSL3)							
CY62128B-SC	4020039	*610028034*	CSPI-R	168	50	0	
STRESS: TC CONDITION C, -65C TO 150C, PRE COND. 192 HRS 30C/60% RH (MSL3)							
CY62128B-SC	4020039	*610028034*	CSPI-R	300	50	0	
CY62128B-SC	4020039	*610028034*	CSPI-R	500	50	0	
CY62128B-SC	4020039	*610028034*	CSPI-R	1000	50	0	