Cypress Semiconductor
Technology Qualification Report

QTP# 99311 VERSION 1.2
December, 2002

R52D-3 Technology, Fab 4 Qualification	
CY7C1329	64K x 32 Synchronous-Pipelined Cache RAM

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

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PRODUCT QUALIFICATION HISTORY

Qual Report	Description of Qualification Purpose	Date Comp
99311	New R52D-3 Technology /New 2Meg,CY7C1329 SRAM device	Aug 99

PRODUCT DESCRIPTION (for qualification)		
Qualification Purpose: To qualify new R52D-3 Technology in Fab 4 and new product CY7C1329.		
Marketing Part #:	CY7C1329	
Device Description:	3.3V, Commercial available in 100-pin TQFP Package.	
Cypress Division:	Cypress Semiconductor Corporation – Memory Product Division (MPD)	
Overall Die (or Mask) REV Level (pre-requisite for qualification):		Rev.D
What ID markings on Die:	7C1329A	

TECHNOLOGY/FAB PROCESS DESCRIPTION – R52D-3			
Number of Metal Layers:	2	Metal Composition:	Metal 1: 500Å TiW/6000Å Al-.5%Cu/300Å TiW Metal 2: 300Å CoTi/8000Å Al-.5%Cu/300Å TiW
Passivation Type and Materials:		1KÅ Oxide + 9KÅ Nitride	
Die Coating(s), if used:		N/A	
Generic Process Technology/Design Rule (µ-drawn):		CMOS, Double Metal /0.25 µm/0.3 FETs	
Gate Oxide Material/Thickness (MOS):		SiO_2 / 55Å	
Name/Location of Die Fab (prime) Facility:		Cypress Semiconductor - Bloomington, MN	
Die Fab Line ID/Wafer Process ID:		Fab4/R52D-3	

PACKAGE	ASSEMBLY FACILITY SITE
100-pin TQFP	**CSPI-R**

Note: Package Qualification details upon request

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	A100
Package Outline, Type, or Name:	100-pin Thin Quad Flat Pack (TQFP)
Mold Compound Name/Manufacturer:	Hitachi CEL9200
Mold Compound Flammability Rating:	V-O per UL 94
Oxygen Rating Index:	>28%
Lead Frame Material:	Copper
Lead Finish, Composition / Thickness:	Solder Plated, 85%Sn, 15%Pb
Die Backside Preparation Method/Metallization:	N/A
Die Separation Method:	Wafer Saw
Die Attach Supplier:	Ablestik
Die Attach Material:	Ablestik 8361H
Bond Diagram Designation	10-03510
Wire Bond Method:	Thermosonic
Wire Material/Size:	1.30um
Thermal Resistance Theta JA °C/W:	51°C/W
Package Cross Section Yes/No:	N/A
Assembly Process Flow:	11-20005
Name/Location of Assembly (prime) facility:	Cypress Philippines (CSPI-R)

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	Cypress Philippines (CSPI-R)
Fault Coverage:	100%

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENTS

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc = 4.5V, 150°C	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc = 3.8V, 150°C	P
High Temperature Steady State Life	Static Operating Condition, Vcc = 3.63V, 150°C	P
High Accelerated Saturation Test (HAST)	140°C, 85%RH, 3.63V Precondition: JESD22 Moisture Sensitivity MSL3 192 Hrs, 30C/60%RH+3IR-Reflow, 220°C+5, -0°C	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity MSL3 192 Hrs, 30C/60%RH+3IR-Reflow, 220°C+5, -0°C	P
Pressure Cooker Test	No bias, 121°C, 100%RH Precondition: JESD22 Moisture Sensitivity MSL3 192 Hrs, 30C/60%RH+3IR-Reflow, 220°C+5, -0°C	P
High Temp Storage	165°C, no bias	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V MIL-STD-883, Method 3015.7	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V Cypress Spec. 25-00020	P
Current Density	Cypress Spec 22-00029	P
Age Bond Pull	MIL-STD-883, Method 2011	P
Acoustic Microscopy/C-SAM	25-00104	P
Latchup Sensitivity	±200mA In accordance with JEDEC 17. Cypress Spec. 01-00081	P

*LTOL done in QTP 99075.

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[4]	Failure Rate
High Temperature Operating Life Early Failure Rate[1]	8317	1	N/A	N/A	120 PPM
High Temperature Operating Life[2,3] Long Term Failure Rate	1,794,740DHRs	3	0.7	170	14 FIT

[1] A production burn-in of 24 Hrs at 150°C, 4.5V is required for the product.
[2] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[3] Chi-squared 60% estimations used to calculate the failure rate.
[4] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A = The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

RELIABILITY TEST DATA

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DEVICE	ASSY-LOC	FABLOT#	ASSYLOT#	DURATION	S/S	REJ	FAIL MODE
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (150C, 4.5V)							
CY7C1329-AC (7C1329D)	CSPI-R	4905886	619909761	48	2988	0	
CY7C1329-AC (7C1329D)	CSPI-R	4905886	619909761	48	1205	0	
CY7C1329-AC (7C1329D)	CSPI-R	4905886	619909776	48	871	0	
CY7C1329-AC (7C1329D)	CSPI-R	4909345	619911324	48	1584	1	1 PARTICLE DEFECT
CY7C1329-AC (7C1329D)	CSPI-R	4909345	619911327	48	1669	0	
STRESS: ESD-CHARGE DEVICE MODEL							
CY7C1329-AC (7C1329D)	CSPI-R	4853292	619902690	1000V	3	0	
CY7C1329-AC (7C1329D)	CSPI-R	4901357	619903817	750V	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015							
CY7C1329-AC (7C1329D)	CSPI-R	4853292	619902690	2200V	3	0	
CY7C1329-AC (7C1329D)	CSPI-R	4901357	619903817	2200V	3	0	
STRESS: STATIC LATCH-UP TESTING (125C, 10V, +/-200mA)							
CY7C1329-AC (7C1329D)	CSPI-R	4853292	619902690	COMP	3	0	
STRESS: HI-ACCEL SATURATION TEST (140C/85%RH/3.63V), PRECOND. 192 HRS 30C/60%RH							
CY7C1329-AC (7C1329D)	CSPI-R	4853292	619902690	128	48	0	
CY7C1329-AC (7C1329D)	CSPI-R	4853292	619902690	256	48	0	
CY7C1329-AC (7C1329D)	CSPI-R	4901357	619903817	128	48	0	
STRESS: HIGH TEMPERATURE STORAGE (165C, NO BIAS)							
CY7C1329-AC (7C1329D)	CSPI-R	4842121	619815465	336	48	0	
CY7C1329-AC (7C1329D)	CSPI-R	4843204	619815797	336	48	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST (150C, 3.63V)							
CY7C1329-AC (7C1329D)	CSPI-R	4842121	619815465	80	80	0	
CY7C1329-AC (7C1329D)	CSPI-R	4842121	619815465	168	80	0	
CY7C1329-AC (7C1329D)	CSPI-R	4843204	619815797	80	80	0	
CY7C1329-AC (7C1329D)	CSPI-R	4843204	619815797	168	80	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (150C, 3.8V)							
CY7C1329-AC (7C1329D)	CSPI-R	4905886	619909761	80	1196	0	
CY7C1329-AC (7C1329D)	CSPI-R	4905886	619909761	500	799	0	
CY7C1329-AC (7C1329D)	CSPI-R	4909345	619911324	80	1491	1	1 UNKNOWN CAUSE
CY7C1329-AC (7C1329D)	CSPI-R	4909345	619911324	500	1199	1	1 UNKNOWN CAUSE
CY7C1329-AC (7C1329D)	CSPI-R	4909345	619911327	80	1640	0	
CY7C1329-AC (7C1329D)	CSPI-R	4909345	619911327	500	1451	1	1 UNKNOWN CAUSE
STRESS: PRESSURE COOKER TEST (121C, 100%RH)							
CY7C1329-AC (7C1329D)	CSPI-R	4853292	619902690	168	48	0	
CY7C1329-AC (7C1329D)	CSPI-R	4901357	619903817	168	46	0	
STRESS: STATIC LATCH-UP TESTING (+/-200 mA)							
CY7C1329-AC (7C1329D)	CSPI-R	4853292	619902690	9.98V	3	0	
CY7C1329-AC (7C1329D)	CSPI-R	4901357	619903817	9.96V	3	0	
STRESS: TC COND. C, -65 TO 150C, PRECOND. 192 HRS 30C/60%RH (MSL 3)							
CY7C1329-AC (7C1329D)	CSPI-R	4842121	619815465	300	48	0	
CY7C1329-AC (7C1329D)	CSPI-R	4842121	619815465	1000	48	0	
CY7C1329-AC (7C1329D)	CSPI-R	4843204	619815797	300	45	0	
CY7C1329-AC (7C1329D)	CSPI-R	4843204	619815797	1000	45	0	