Cypress Semiconductor
Technology Qualification Report

QTP# 99285 VERSION 1.5
November 2008

L28-TSMC Technology in TSMC-2A, Taiwan

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

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TECHNOLOGY QUALIFICATION HISTORY

Qual Report		Description of Qualification Purpose		Date Comp
99285		To qualify L28-TSMC Technology in TMSC-2A		May 2003

PRODUCT DESCRIPTION (for qualification)	
Qualification Purpose: To qualify L28-TSMC Technology in TMSC-2A	
Marketing Part #:	CY2280PVC
Package:	48 pins SSOP
Device Description:	100-MHz Pentium ® II Clock Synthesizer/Driver with Spread Spectrum for Mobile or Desktop PCs
Cypress Division:	Cypress Semiconductor Corporation - CPD Division
Overall Die (or Mask) REV:	Rev. A
What ID markings on Die:	7C83760A

TECHNOLOGY/FAB PROCESS DESCRIPTION - L28			
Number of Metal Layers:	2	Metal Composition:	Metal 1: Ti 400A /TiN1000A /AlSiCu 4700A /TiN 375A Metal 2: Ti 1500A/ AlSiCu 8000A/ TiN 375A
Passivation Type and Materials:		SiN 3000A/SOG 3150A/SiN 12000A	
Generic Process Technology/Design Rule(µ-drawn):		CMOS, Single Poly, Double Metal /0.65 µm	
Gate Oxide Material/Thickness (MOS):		SiO_2 / 125 A	
Name/Location of Die Fab (prime) Facility:		TSMC-2A, Taiwan	
Die Fab Line ID/Wafer Process ID:		TSMC-2A /L28-TSMC	

PLASTIC PACKAGE/ASSEMBLY DESCRIPTION			
Package Outline, Type, or Name:	48 Pins SSOP		
Mold Compound Name/Manufacturer:	Hitachi CEL-9200		
Lead Frame material:	Copper/ C7025		
Lead Finish, composition:	Solder Plated, 40%Sn, 10%Pb		
Die Attach Area Plating:	Silver	Die Attach Pad Size:	130 x 160 mil
Die Attach Method:	Epoxy	Die Attach Material:	Ablestik 8361/H
Wire Bond Method:	Thermosonic	Wire Material/Size:	Gold / 1.0 mil
Thermal Resistance JA:	55		
JESD22-A112 Moisture Sensitivity Level	Level 1 (previously qualified)		
Assembly Line ID and Process ID:	Cypress Philippines (CSPI-R)		

Note: Please contact a Cypress Representative for other packages availability.

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc = 3.8V, 150°C	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc = 3.8V, 150°C	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65C to 150C Precondition: JESD22 Moisture Sensitivity Level 1 (168 hrs, 85C/85%RH)	P
High Accelerated Saturation Test (HAST)	130C, 3.63V, 85%RH Precondition: JESD22 Moisture Sensitivity Level 1 (168 Hrs, 85C/85%RH)	P
High Temperature Steady Life Test	Cypress Spec. 29-00020 (VCC=150C/3.63V)	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V MIL-STD-883, Method 3015.7	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	1,000V Cypress Spec. 25-00020	P
Low Temperature Operating Life	Cypress Spec. 25-00089 (-30C)	P
Pressure Cooker	Cypress Spec. 25-00047 (121C/100%RH)	P
Data Retention	Cypress Spec. 25-00060 (150C)	P
Age Bond	MIL-STD-883, Method 2011	P
SEM	MIL-STD-883, Method 2018-2	P
Latchup Sensitivity	I10 V,± 200mA In accordance with JEDEC 17. Cypress Spec. 01-00081	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Acceleration Factor[3]	Failure Rate
High Temperature Operating Life Early Failure Rate	1019	0	N/A	N/A	0 PPM
High Temperature Operating Life[1, 2] Long Term Failure Rate	181,660HRs	0	0.7	170	30FIT

[1] Assuming an ambient temperature of 150°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate.
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

Reliability Test Data

QTP #: 99285

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: DATA RETENTION, PLASTIC, 150C							
CY2280-OC	2937109	619927291/2/3	CSPI-R	500	85	0	
CY2280-OC	2937109	619927291	CSPI-R	500	85	0	
CY2280-OC	2937109	619927291	CSPI-R	1000	85	0	
CY2280-OC	2937190	619928659	CSPI-R	500	50	0	
CY2280-OC	2937190	619928659	CSPI-R	1000	50	0	
CY2280-OC	2942829	619933793	CSPI-R	500	50	0	
CY2280-OC	2942829	619933793	CSPI-R	1000	50	0	
STRESS: ESD-CHARGE DEVICE MODEL, (1000V)							
CY2280-OC	2937109	619927291/2/3	CSPI-R	COMP	3	0	
CY2280-OC	2937190	619928659/60/61	CSPI-R	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER PER MIL STD 883, METHOD 3015 (2,200V)							
CY2280-OC	2937109	619927291/2/3	CSPI-R	COMP	3	0	
CY2280-OC	2937190	619928659/60/61	CSPI-R	COMP	3	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (150C, 3.8V, Vcc Max)							
CY2280-OC	2937109	619927291/2/3	CSPI-R	48	335	0	
CY2280-OC	2937190	619928659/60/61	CSPI-R	48	234	0	
CY2280-OC	2937190	619928659/60/61	CSPI-R	48	101	0	
CY2280-OC	2942829	619933793/4/5	CSPI-R	48	349	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (150C, 3.8V, Vcc Max)							
CY2280-OC	2937109	619927291/2/3	CSPI-R	80	120	0	
CY2280-OC	2937109	619927291/2/3	CSPI-R	500	120	0	
CY2280-OC	2937190	619928659/60/61	CSPI-R	80	120	0	
CY2280-OC	2937190	619928659/60/61	CSPI-R	500	120	0	
CY2280-OC	2942829	619933793/4/5	CSPI-R	80	125	0	
CY2280-OC	2942829	619933793/4/5	CSPI-R	500	123	0	
STRESS: HI-ACCEL SATURATION TEST (140C/85%RH/3.63V), PRECOND. 168 HRS 85C/85%RH							
CY2280-OC	2937109	619927291/2/3	CSPI-R	128	50	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST (150C, 3.63V)							
CY2280-OC	2937109	619927291/2/3	CSPI-R	80	77	0	
CY2280-OC	2937109	619927291/2/3	CSPI-R	168	77	0	

Reliability Test Data

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Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: LOW TEMPERATURE OPERATING LIFE (-30C/8MHZ)							
CY2280-OC	2937190	619928659/60/61	CSPI-R	500	50	0	
STRESS: PRESSURE COOKER TEST, MSL 1 (121C, 100%RH)							
CY2280-OC	2937109	619927291/2/3	CSPI-R	168	53	0	
STRESS: TC COND. C, -65 TO 150C, PRECOND. 168 HRS 85C/85%RH (MSL 1))							
CY2280-OC	2937109	619927291/2/3	CSPI-R	300	50	0	