Cypress Semiconductor
Technology Qualification Report

QTP# 99273 VERSION 2.0
August, 2003

P26 Technology with Triple Layer Metal in Fab 2

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

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PRODUCT/TECHNOLOGY INFORMATION

PRODUCT DESCRIPTION (for qualification)		
Purpose: Qualify: Triple Layer Metal, P26 Process Technology in Fab2. (Device with triple layer metal will be qualified separately).		
Device Description:	Test Chip with Triple Metal Layer	
Cypress Division:	Cypress Semiconductor Corporation - CPD Division	
Overall Die (or Mask) REV Level (pre-requisite for qualification):		Rev. A
What ID markings on Die:	7C6399A	

TECHNOLOGY/FAB PROCESS DESCRIPTION			
Number of Metal Layers:	3	Metal Composition:	Metal 1: 6000Å Al, 1200 Å TiW Metal 2: 1500Å TiW, 9000Å Al, 320Å TiW Metal 3: 320 ÅTiW/10000 ÅAl/1500Å TiW
Generic Process Technology/Design Rule (µ-drawn):		Triple Metal / 0.65µm	
Gate Oxide Material/Thickness (MOS):		SiO_2 / 65 Å	
Name/Location of Die Fab (prime) Facility:		Cypress Semiconductor - Round Rock, TX (Fab2)	
Die Fab Line ID/Wafer Process ID:		Fab 2/ P26TLM	

PLASTIC PACKAGE/ASSEMBLY DESCRIPTION			
Package Outline, Type, or Name:	20-pin PDIP/24-pin SOIC		
Mold Compound Name/Manufacturer:	Nitto MP-8000/Sumitomo EME-6300		
Lead Frame material:	Copper		
Lead Finish, composition:	Solder Plate, 85%Pb /155%Sn		
Die Attach Area Plating:	Silver Spot	Die Attach Pad Size:	180 x 180 mils
Die Attach Method:	Epoxy	Die Attach Material:	Ablestik 8361
Wire Bond Method:	Thermosonic	Wire Material/Size:	Au / 1.0mil
Assembly Line Process Flow:	49-24009		
Thermal Resistance Theta JA °C/W	74/79°C/W		
JESD22-A112 Moisture Sensitivity Level	Level 1		
Assembly Line ID and Process ID:	Indonesia (OMEDATA) Cypress Philippines (CSPI-R)		

Note: Please contact a Cypress Representative for other packages availability.

RELIABILITY TESTS PERFORMED

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc = 5.75V, 150°C	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc = 5.75V, 150°C	P
High Accelerated Saturation Test (HAST)	130°C/140°/5.5V, 85%RH Precondition: JESD22 Moisture Sensitivity Level 1 168 Hrs, 85°C/85%RH	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity Level 1 (168 hrs, 85°C/85%RH)	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V MIL-STD-883, Method 3015.7	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V Cypress Spec. 25-00020	P
High Temperature Storage	16°5C, No Bias	P
Data Bake Plastic	Cypress Spec. 25-00060 (165°C, No Bias)	P
Long Life Verification	Cypress Spec. 29-00020 (150°C/5.75V)	P
Pressure Cooker	Cypress Spec. 25-00047 (121°C/100%RH)	P
Age Bond	MIL-STD-883, Method 2011	P
Acoustic Microscopy	Cypress Spec 25-000104	P
SEM	MIL-STD-883, Method 2018-2	P
Dynamic Latch-up	9.5V In accordance with JEDEC 17. Cypress Spec. 01-00081	P
Static Latch-up	11.5V, +/-300mA In accordance with JEDEC 17. Cypress Spec. 01-00081	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Acceleration Factor[3]	Failure Rate[4]
High Temperature Operating Life Early Failure Rate	3598	0	N/A	N/A	0 PPM
High Temperature Operating Life[1,2] Long Term Failure Rate	189,600 DHRs	0	0.7	170	28 FIT

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate.
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

Where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

[4] The P26 technology was qualified in Fab2 with a Fit Rate of 14 - 398,000 DHRs. with 0 reject, QTP # 96411, 96352, 95517 and 95075.

RELIABILITY TEST DATA

QTP#: 99273

DEVICE	ASSY-LOC	FABLOT#	ASSYLOT#	DURATION	S/S	REJ	FAIL MODE
STRESS: DATA BAKE-PLASTIC (165C, NO BIAS)							
7C6399AT	CSPI-R	2920309	619918583	168	78	0	
7C6399AT	CSPI-R	2920309	619918583	552	78	0	
7C6399AT	CSPI-R	2931408	619927766	168	81	0	
7C6399AT	CSPI-R	2931408	619927766	552	81	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (150C, 5.75V)							
7C6399AT	INDNS-O	2920309	519911818/19/20	48HRS	978	0	
7C6399AT	CSPI-R	2931408	519915664/5756/	48	1000	0	
7C6399AT	CSPI-R	2931408	519915664/5756/	48	520	0	
7C6399AT	CSPI-R	2920309	619918583	48	1100	0	
STRESS: ESD-CHARGE DEVICE MODEL (1000V)							
7C6399AT	CSPI-R	2920309	619918583	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015 (2200V)							
7C6399AT	CSPI-R	2920309	619918583	COMP	3	0	
STRESS: HI-ACCEL SATURATION TEST (140C/85%RH/5.5V), PRECOND. 168 HRS 85C/85%RH							
7C6399AT	CSPI-R	2920309	619918583	128	50	0	
7C6399AT	CSPI-R	2931408	619927766	128	49	0	
STRESS: HIGH TEMPERATURE STORAGE (165C, NO BIAS)							
7C6399AT	CSPI-R	2920309	619918583	336	46	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (150C, 5.75V)							
7C6399AT	INDNS-O	2920309	519911818/19/20	80	120	0	
7C6399AT	INDNS-O	2920309	519911818/19/20	500	120	0	
7C6399AT	CSPI-R	2931408	519915664/5756/	80	120	0	
STRESS: EXTENDED DYNAMIC BURN-IN (150C, 5.75V)							
7C6399AT	CSPI-R	2920309	619918583	1000	120	0	
STRESS: PRESSURE COOKER TEST (121C, 100%RH)							
7C6399AT	CSPI-R	2920309	619918583	168	47	0	
STRESS: TC COND. C, -65 TO 150C, PRECOND. 168 HRS 85C/85%RH (MSL 1)							
7C6399AT	CSPI-R	2920309	619918583	300	45	0	