

# Cypress Semiconductor Qualification Report

QTP# 99175 VERSION 1.0  
October, 1999

<b>Military Clocked FIFOs – R28 Technology – Fab2</b>	
<b>CY7C441/443</b>	<b>512/2K x 9 Clocked FIFO</b>
<b>CY7C451/453/454</b>	<b>512/2K/4K x 9 Cascadable Clocked FIFO With Programmable Flags</b>

**CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:**

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Reliability Manager  
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<b>PRODUCT DESCRIPTION (for qualification)</b>			
Qualification Purpose: to qualify CY7C454 (Rev. B) and the options for military, R28 technology, Fab2. The commercial products QTP 98312.			
Marketing Part #:	CY7C454		
Package:	32L Ceramic Leadless Chip Carrier		
Device Description:	4K x 9 Cascadable Clocked FIFO		
Cypress Division:	Cypress Semiconductor Corporation – DCD Division		
Overall Die (or Mask) REV Level (pre-requisite for qualification):	Rev. B		
Die Size (stepping):	112 mils x 159 mils	What ID markings on Die:	7C453A

<b>TECHNOLOGY/FAB PROCESS DESCRIPTION - R28</b>			
Number of Metal Layers:	2	Metal Composition:	Metal 1: Ti/TiW/Al-Si/TiW, 500Å/1.2KÅ/6KÅ/1.2K Å Metal 2: TiW/Al-Si/TiW, 1.2KÅ/10KÅ/150Å
Passivation Type and Materials:	7000A TEOS + 6000A Si <sub>2</sub> N <sub>4</sub>		
Free Phosphorus contents in top glass layer(%):	N/A		
Die Coating(s), if used:	None		
Generic Process Technology/Design Rule (μ-drawn):	CMOS, Double Poly, Double Metal /0.65 μm		
Gate Oxide Material/Thickness (MOS):	SiO <sub>2</sub> / 165 Å		
Name/Location of Die Fab (prime) Facility:	Cypress Semiconductor - Round Rock, TX		
Die Fab Line ID/Wafer Process ID:	Fab2/R28		

<b>HERMETIC PACKAGE/ASSEMBLY DESCRIPTION</b>			
Package Outline, Type, or Name:	32L Ceramic Leadless Chip Carriers		
Lid Seal Method / Material:	Solder Gold Eutectic		
Lead Finish, composition:	Solder Dip, 63%Sn, 37%Pb		
Die Attach Method:	Ag Glass	Die Attach Material:	Silver Glass
Wire Bond Method:	Ultrasonic	Wire Material/Size:	Al / 1.25 mil
Assembly Line ID and Process ID:	Alphatec, Thailand		

**Note:** Please contact a Cypress Representative for other packages availability.

**RELIABILITY TESTS PERFORMED**

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc = 5.75V, 150°C	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc = 5.75V, 150°C	P
Group C, Military Life Test	Mil-Std-883, Method 1005.4, Vcc = 5.75V, 150°C	P
Temp Cycle, Hermetic	Mil-Std-883, Method 1001, Condition C	P
Electrostatic Discharge Human Body Model (ESD-HBM)	MIL-STD-883, Method 3015.7	2200V
Electrostatic Discharge Charge Device Model (ESD-CDM)	Cypress Spec. 25-00020	1000V
Latchup Sensitivity	In accordance with JEDEC 17. Cypress Spec. 01-00081	P 12.0V ± 200 mA

**RELIABILITY FAILURE RATE SUMMARY**

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF <sup>3</sup>	Failure Rate <sup>4</sup>
High Temperature Operating Life Early Failure Rate <sup>5</sup>	2610 Devices (Com. & Mil. Quals)	0	N/A	N/A	0 PPM
High Temperature Operating Life <sup>1,2</sup> Long Term Failure Rate	68,832 DHRs (Com. & Mil. Quals)	0	0.7	170	78 FIT

<sup>1</sup> Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.

<sup>2</sup> Chi-squared 60% estimations used to calculate the failure rate.

<sup>3</sup> Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp \left[ \frac{E_A}{k} \left[ \frac{1}{T_2} - \frac{1}{T_1} \right] \right]$$

where:

E<sub>A</sub> = The Activation Energy of the defect mechanism.

k = Boltzmann's constant = 8.62x10<sup>-5</sup> eV/Kelvin.

T<sub>1</sub> is the junction temperature of the device under stress and T<sub>2</sub> is the junction temperature of the device at use conditions.

<sup>4</sup> The Clocked FIFO, R28 Technology was qualified in Fab3 with a Fit rate of 28, QTP 96154.

<sup>5</sup> Production burn-in of 80 hours, 150C, 6.5V is required for the product.

**RELIABILITY TEST DATA**

**QTP#: 99175**

<b>DEVICE</b>	<b>ASSY-LOC</b>	<b>FABLOT#</b>	<b>ASSYLOT#</b>	<b>DURATION</b>	<b>S/S</b>	<b>REJ</b>	<b>FAIL MODE</b>
<b>STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (150C, 5.75V)</b>							
CY7C454-LMB	ALPHA-X	2907136	619911754	48	175	0	
CY7C454-LMB	ALPHA-X	2907136	619911754	48	660	0	
CY7C454-LMB	ALPHA-X	2907136	619911754	48	180	0	
<b>STRESS: ESD-CHARGE DEVICE MODEL (1000V)</b>							
CY7C454-LMB	ALPHA-X	2907136	619911754	COMP	3	0	
<b>STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015 (2200V)</b>							
CY7C454-LMB	ALPHA-X	2907136	619911754	COMP	3	0	
<b>STRESS: GROUP C, SUBGROUP 1 LIFE TEST MIL-STD-883, METHOD 1005.4 (150C, 5.75V)</b>							
CY7C454-LMB	ALPHA-X	2907136	619911754	184	48	0	
<b>STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (150C, 5.75V)</b>							
CY7C454-LMB	ALPHA-X	2907136	619911754	80	120	0	
CY7C454-LMB	ALPHA-X	2907136	619911754	500	120	0	
<b>STRESS: TC COND. C, -65 TO 150C, HERMETIC DEVICES</b>							
CY7C454-LMB	ALPHA-X	2907136	619911754	100	48	0	
CY7C454-LMB	ALPHA-X	2907136	619911754	1000	48	0	

**RELIABILITY TEST DATA**

**QTP#: 98312<sup>1</sup>**

DEVICE	ASSY-LOC	FABLOT#	ASSYLOT#	DURATION	S/S	REJ	FAIL MODE
<b>STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (150C, 5.75V)</b>							
CY7C457-JC	INDNS-O	2823136	519809904S1	48	889	0	
CY7C457-JC	INDNS-O	2823136	519809904S1	48	111	0	
<b>STRESS: ESD-CHARGE DEVICE MODEL (750V)</b>							
CY7C457-JC	INDNS-O	2823136	519809904S1	COMP	3	0	
<b>STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015 (2,200V)</b>							
CY7C457-JC	INDNS-O	2823136	519809904S1	COMP	3	0	

<sup>1</sup> QTP 98312, Commercial Clocked FIFO, R28 Technology, Fab2 qualification.