Cypress Semiconductor
Qualification Report

QTP# 99011 VERSION 1.0
April, 1999

256K Static RAM, R28 Technology, Fab 2	
CY7C191/192	64K x 4 Static RAM With Separate I/O
CY7C194/195/196	64K x 4 Static RAM
CY7C197	256K x 1 Static RAM
CY7C199	32K x 9 Static RAM

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

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Reliability Manager
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PRODUCT DESCRIPTION (for qualification)	
Qualification Purpose: To qualify CY7C192 Rev. H and options to be fabricated in Fab2, R28 Technology	
Marketing Part #:	CY7C192
Package:	28 pins, 300 mil SOJ
Device Description:	64K x 4 Static RAM With Separate I/O
Cypress Division:	Cypress Semiconductor Corporation - MPD Division
Overall Die (or Mask) REV Level (pre-requisite for qualification):	Rev. H
What ID markings on Die:	7C191/2

TECHNOLOGY/FAB PROCESS DESCRIPTION - R28			
Number of Metal Layers:	2	Metal Composition:	Metal 1: Ti/TiW/Al-Si/TiW, 500Å/1.2KÅ/6KÅ/1.2K Å Metal 2: TiW/Al-Si/TiW, 1.2KÅ/10KÅ/150Å
Passivation Type and Materials:	7000A TEOS + 6000A Si_2N_4		
Free Phosphorus contents in top glass layer(%):	N/A		
Die Coating(s), if used:	None		
Generic Process Technology/Design Rule (μ-drawn):	CMOS, Double Poly, Double Metal /0.65 μm		
Gate Oxide Material/Thickness (MOS):	SiO_2 / 165 Å		
Name/Location of Die Fab (prime) Facility:	Cypress Semiconductor - Round Rock, TX		
Die Fab Line ID/Wafer Process ID:	Fab2/R28		

PLASTIC PACKAGE/ASSEMBLY DESCRIPTION			
Package Outline, Type, or Name:	28-pin, 300 mil SOJ		
Mold Compound Name/Manufacturer:	Hitachi CEL9200		
Lead Frame material:	Copper Alloy 194		
Lead Finish, composition:	Solder Plated, 85%Sn, 15%Pb		
Die Attach Area Plating:	Silver Spot		
Die Attach Method:	Paste	Die Attach Material:	Ablestik 8361
Wire Bond Method:	Thermosonic	Wire Material/Size:	Gold / 1.0 mil
JESD22-A112 Moisture Sensitivity Level	Level 1 (previously qualified)		
Assembly Line ID and Process ID:	Alphatec, Thailand (ALPHA-X)		

Note: Please contact a Cypress Representative for other packages availability.

RELIABILITY TESTS PERFORMED

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc = 5.75V, 150°C	P
Electrostatic Discharge Human Body Model (ESD-HBM)	MIL-STD-883, Method 3015.7	2,200V
Electrostatic Discharge Charge Device Model (ESD-CDM)	Cypress Spec. 25-00020	500V
Latchup Sensitivity	In accordance with JEDEC 17. Cypress Spec. 01-00081	11.2V ±200mA

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[4]	Failure Rate[5]
High Temperature Operating Life Early Failure Rate[1]	1690	0	N/A	N/A	0 PPM
High Temperature Operating Life[2,3] Long Term Failure Rate	122,500 DHRs	0	0.7	170	44 FIT

[1] Production burn-in of 20 hrs. at 125C, 7V is required for the product.
[2] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[3] Chi-squared 60% estimations used to calculate the failure rate.
[4] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A = The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

[5] **Long Term Failure rate is based on 8K x 18 DP SRAM (CY7C0251, rev. D), R28 technology, Fab 2 qualification, QTP 98302.**

RELIABILITY TEST DATA

QTP#: 99011

DEVICE	ASSY-LOC	FABLOT#	ASSYLOT#	DURATION	S/S	REJ	FAIL MODE
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (150C, 5.75V)							
CY7C192-VC	ALPHA-X	2834955	219808135N	48	616	0	
CY7C192-VC	ALPHA-X	2831719	219808300	48	874	0	
STRESS: ESD-CHARGE DEVICE MODEL (500V)							
CY7C192-VC	ALPHA-X	2834955	219807135N	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015 (2200V)							
CY7C192-VC	ALPHA-X	2834955	219807135N	COMP	3	0	

DEVICE RELATED RELIABILITY TEST DATA

QTP#: 98302[1]

DEVICE	ASSY-LOC	FABLOT#	ASSYLOT#	DURATION	S/S	REJ	FAIL MODE
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (150C, 5.75V)							
CY7C0251-AC	KOREA-Q	2824171	619809165	48	536	0	
CY7C0251-AC	KOREA-Q	2824171	619809165	48	125	0	
CY7C0251-AC	KOREA-Q	2824171	619809165	48	467	0	
CY7C0251-AC	KOREA-Q	2824171	619809165	48	505	0	
CY7C0251-AC	KOREA-Q	2828426	619810549	48	509	1	1 UNKOWN
STRESS: ESD-CHARGE DEVICE MODEL (1000V)							
CY7C0251-AC	KOREA-Q	2824171	619809165	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015 (2,200V)							
CY7C0251-AC	KOREA-Q	2824171	619809165	COMP	3	0	
STRESS: HI-ACCEL SATURATION TEST (140C, 5.5V), PRECOND. 192 HRS 30C/60%RH							
CY7C0251-AC	KOREA-Q	2824171	619809165	128	45	0	1 EOS
STRESS: HI-ACCEL SATURATION TEST (140C, 5.5V), PRECOND. DB + 72 HRS 30C/60%RH							
CY7C0251-AC	KOREA-Q	2824171	619809165	128	47	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (150C, 5.75V)							
CY7C0251-AC	KOREA-Q	2824171	619809165	80	125	0	
CY7C0251-AC	KOREA-Q	2824171	619809165	500	125	0	
CY7C0251-AC	KOREA-Q	2828426	619810549	80	120	0	
CY7C0251-AC	KOREA-Q	2828426	619810549	500	120	0	
STRESS: PRESSURE COOKER TEST (121C, 100%RH)							
CY7C0251-AC	KOREA-Q	2824171	619809165	168	47	0	
STRESS: TC COND. C, -65 TO 150C, PRECOND. 72 HRS 30/60%RH (MSL 5)							
CY7C0251-AC	KOREA-Q	2824171	619809165	300	47	0	
CY7C0251-AC	KOREA-Q	2828426	619810548	300	50	0	
CY7C0251-AC	KOREA-Q	2828426	619810549	300	50	0	
CY7C0251-AC	KOREA-Q	2828426	619810549	1000	50	0	

[1] QTP 98302, DP SRAM, R28 Technology, qualified in Fab 2.