

Cypress Semiconductor Qualification Report

QTP# 98081 VERSION 2.0
August, 1999

Synchronous 3.3V Cache RAM R42D Technology w/ Hot Al, Fab 4 Qualification	
CY7C1325	256K x 18 Synchronous Cache RAM
CY7C1327	256K x 18 Synchronous Pipelined Cache RAM
CY7C1345	128K x 36 Synchronous Flow-Through Cache RAM
CY7C1347	128K x 36 Synchronous Pipelined Cache RAM
CY7C1338	128K x 32 Synchronous Flow-Through Cache RAM
CY7C1339	128k x 32 Synchronous Pipelined Cache RAM

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

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Reliability Manager
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PRODUCT DESCRIPTION (for qualification)	
Qualification Purpose: Qualifies 256K x 18 Synchronous 3.3V Cache RAM, CY7C1325 and its options in R42D technology with Hot Al in Fab4.	
Marketing Part #:	CY7C1325
Package:	100-pin TQFP
Device Description:	256K x 18 Synchronous Cache RAM
Cypress Division:	Cypress Semiconductor Corporation - MPD Division
Overall Die (or Mask) REV Level (pre-requisite for qualification):	Rev. A
What ID markings on Die:	7C1325A

TECHNOLOGY/FAB PROCESS DESCRIPTION - R42D			
Number of Metal Layers:	2	Metal Composition:	Metal 1: TiW,AlCu,TiW/500Å,6000Å,1200Å Metal 2: TiW,AlCu,TiW/500Å,8000Å,300Å
Passivation Type and Materials:	3000Å SiO ₂ + 6000Å Si ₃ N ₄		
Free Phosphorus contents in top glass layer(%):	0%		
Die Coating(s), if used:	None		
Generic Process Technology/Design Rule (μ-drawn):	CMOS, Double Metal /0.35 μm		
Gate Oxide Material/Thickness (MOS):	SiO ₂ / 70 Å		
Name/Location of Die Fab (prime) Facility:	Cypress Semiconductor - Bloomington, MN		
Die Fab Line ID/Wafer Process ID:	Fab4/R42D w/ Hot Al		

PLASTIC PACKAGE/ASSEMBLY DESCRIPTION			
Package Outline, Type, or Name:	100-pins TQFP		
Mold Compound Name/Manufacturer:	Hitachi CEL9200		
Lead Frame material:	Copper		
Lead Finish, composition:	Solder Plated, 90%Sn, 10%Pb		
Die Attach Area Plating:	Silver Spot		
Die Attach Method:	Epoxy	Die Attach Material:	Ablestik 8361H
Wire Bond Method:	Thermosonic	Wire Material/Size:	Gold / 1.0 mil
JESD22-A112 Moisture Sensitivity Level:	Level 3		
Name/Location of Assembly (prime) facility:	Cypress Philippines (CSPI-R)		

Note: Please contact a Cypress Representative for other packages availability.

RELIABILITY TESTS PERFORMED

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc = 3.8 V, 150°C	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc = 3.8 V, 150°C	P
High Temperature Steady State Life	Static Operating Condition, Vcc = 3.63V, 150°C	P
High Accelerated Saturation Test (HAST)	140°C, 3.65V Precondition: JESD22 Moisture Sensitivity Level 3 (192 Hrs, 30/60% RH)	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity Level 3 (192 Hrs, 30C/60%RH)	P
Electrostatic Discharge Human Body Model (ESD-HBM)	MIL-STD-883, Method 3015.7	4,400V
Electrostatic Discharge Charge Device Model (ESD-CDM)	Cypress Spec. 25-00020	500V
Latchup Sensitivity	In accordance with JEDEC 17. Cypress Spec. 01-00081	9.0V
Pressure Cooker Test	No bias, 121°C, 100%RH	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF ⁴	Failure Rate
High Temperature Operating Life Early Failure Rate ¹	1722	0	N/A	N/A	0 PPM
High Temperature Operating Life ^{2,3} Long Term Failure Rate	455,500	0	0.7	170	12 FIT

¹ A production burn-in of 24 Hrs at 150°C, 4.3V is required for the product.

² Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.

³ Chi-squared 60% estimations used to calculate the failure rate.

⁴ Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp \left[\frac{E_A}{k} \left[\frac{1}{T_2} - \frac{1}{T_1} \right] \right]$$

where:

E_A = The Activation Energy of the defect mechanism.

k = Boltzmann's constant = 8.62x10⁻⁵ eV/Kelvin.

T₁ is the junction temperature of the device under stress and T₂ is the junction temperature of the device at use conditions.

RELIABILITY TEST DATA

QTP#: 98081

DEVICE	ASSY-LOC	FABLOT#	ASSYLOT#	DURATION	S/S	REJ	FAIL MODE
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (150C, 3.8V)							
CY7C1325-AC	CSPI-R	4812402	619805641	48	120	0	
CY7C1325-AC	CSPI-R	4816671	619806417	48	850	0	
CY7C1325-AC	CSPI-R	4819957	619807576	48	752	0	2 Electrical Overstress
STRESS: ESD-CHARGE DEVICE MODEL (500V)							
CY7C1325-AC	CSPI-R	4816671	619806417	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015 (4,400V)							
CY7C1325-AC	CSPI-R	4816671	619806417	COMP	3	0	
STRESS: HI-ACCEL SATURATION TEST (140C, 3.65V), PRECOND. 192 HRS 30C/60%RH							
CY7C1325-AC	CSPI-R	4812402	619805641	128	47	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST (150C, 5.63V)							
CY7C1325-AC	CSPI-R	4812402	619805641	80	78	0	
CY7C1325-AC	CSPI-R	4812402	619805641	168	78	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (150C, 3.8V)							
CY7C1325-AC	CSPI-R	4812402	619805641	80	120	0	
CY7C1325-AC	CSPI-R	4812402	619805641	500	120	0	
CY7C1325-AC	CSPI-R	4816671	619806417	80	396	0	
CY7C1325-AC	CSPI-R	4816671	619806417	500	396	0	
CY7C1325-AC	CSPI-R	4819957	619807576	80	396	0	1 Electrical Overstress
CY7C1325-AC	CSPI-R	4819957	619807576	500	395	0	
STRESS: PRESSURE COOKER TEST (121C, 100%RH)							
CY7C1325-AC	CSPI-R	4816671	619806417	168	48	0	(See Note 1)
STRESS: TC COND. C, -65 TO 150C, PRECOND. 192 HRS 30C/60%RH (MSL 3)							
CY7C1325-AC	CSPI-R	4812402	619805641	300	48	0	
CY7C1325-AC	CSPI-R	4819957	619807575	300	48	0	
CY7C1325-AC	CSPI-R	4819957	619807576	300	48	0	
STRESS: TC COND. C, -65 TO 150C, PRECOND. 168 HRS 85C/85%RH (MSL 1)							
CY7C1338-AC***	CSPI-R	4903616	619907235	300	333	0	
CY7C1338-AC***	CSPI-R	4903616	619907235	500	333	2	2 Unknown cause
CY7C1338-AC***	CSPI-R	4903616	619907235	1000	331	0	

*** Reliability Monitor data, R992308.

Note1: 1 Topside defect due to mechanical damaged. The reject was not QTP related.