Cypress Semiconductor
Qualification Report

QTP# 97222VERSION 1.0
December, 1997

ASYNCHRONOUS FIFOs - R3.2D TECHNOLOGY	
CY7C466A	64K x 9 Asynchronous FIFOs
CY7C464A	32K x 9 Asynchronous FIFOs
CY7C462A	16K x 9 Asynchronous FIFOs
CY7C460A	8K x 9 Asynchronous FIFOs

PRODUCT DESCRIPTION			
Information provided in this document is intended for generic qualification and technically describes the Cypress part supplied: CY7C466C/CY7C464C/CY7C462C/CY7C460C			
Marketing Part #:	CY7C466C		
Package:	68-Lead PLCC		
Device Description:	64K x 9 Synchronous FIFOs		
Cypress Division:	Cypress Semiconductor Corporation - DCD Division		
Overall Die (or Mask) REV Level (pre-requisite for qualification):		Rev. C	
Die Size (stepping):	131 mils x 250 mils	What ID markings on Die:	7C466B

TECHNOLOGY/FAB PROCESS DESCRIPTION - R32D			
Number of Metal Layers	2	Metal Composition	Metal 1: Al-Cu/TiW Metal 2: TiW/Al-Cu/TiW
Passivation Type and Materials:		Silicon Dioxide 7,000Å + Silicon Nitride 6,000Å	
Number of Transitors in device		4,000,000	
Number of Gates in devices		125,000	
Free Phosphorus contents in top glass layer(%):		0%	
Die Coating(s), if used:		N/A	
Generic Process Technology/Design Rule (µ-drawn):		CMOS, Single Local Interconnect, Double Metal /0.5 µm	
Gate Oxide Material/Thickness (MOS):		SiO_2 / 145Å	
Name/Location of Die Fab (prime) Facility:		Cypress Semiconductor - Bloomington, MN	
Die Fab Line ID/Wafer Process ID		Fab4/R32D	

PLASTIC PACKAGE/ASSEMBLY DESCRIPTION			
Package Outline, Type, or Name	68-Lead PLCC		
Mold Compound Name/Manufacturer:	Nitto 8000CH (PLCC)		
Lead Frame material:	Copper		
Die Coatings (if used):	None		
Lead Finish, composition	Solder Plated, 85%Sn, 15%Pb		
Die Attach Area Plating:	Silver Spot		
Die Attach Method	Paste	Die Attach Material:	Ablestik 8361H
Wire Bond Method	Thermosonic	Wire Material/Size:	Gold / 1.3 mil
JESD22-A12 Moisture Sensitivity Level	Level 3		
Name/Location of Assembly (prime) facility:	Cypress Bangkok, Thailand (ALPHA-X)		

Note: Please contact a Cypress Representative for other packages availability.

RELIABILITY TESTS PERFORMED

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc = 5.75V, 150°C	P
High Temperature Steady State Life	Static Operating Condition, Vcc = 5.75V, 150°C	P
Read and Record	Dynamic Operating Condition, Vcc = 5.75V, 150°C	P
High Accelerated Saturation Test (HAST)	140°C, 85%RH, 5.5V bias Precondition: JESD22 Moisture Sensitivity Level 3 (192 Hrs. 30°C/60%RH)	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity Level 3 (192 Hrs. 30°C/60%RH)	P
Electrostatic Discharge Human Body Model (ESD-HBM)	MIL-STD-883, Method 3015.7	4,400V
Electrostatic Discharge Charge Device Model (ESD-CDM)	Cypress Spec. 25-00020	2000V
Alpha Particle Sensitivity	Cypress Spec 2	
Latchup Sensitivity Dynamic Latchup Static Latchup	In accordance with JEDEC 17. Cypress Spec. 01-00081	P 8.2V 11.4V

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[4]	Failure Rate
High Temperature Operating Life Early Failure Rate	NA[3]	NA	N/A	N/A	NA
High Temperature Operating Life[1,2] Long Term Failure Rate	400,000 DHRs	0	0.6	170	13 FIT

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate.
[3] Early Failure Rate was not performed. A production burn-in of 80 Hrs., 150°C, 6.5V is performed for the device.
[4] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A = The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

RELIABILITY TEST DATA

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DEVICE	ASSY-LOC	FABLOT#	ASSYLOT#	DURATION	S/S	REJ	FAIL MODE
STRESS: ESD-CHARGE DEVICE MODEL (2,000V)							
CY7C466A-JC	ALPHA-X	4723663	219709366	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015 (4,400V)							
CY7C466A-JC	ALPHA-X	4723663	219709366	COMP	3	0	
STRESS: HI-ACCEL SATURATION TEST (140C, 5.5V), PRECOND. 192 HRS 30C/60%RH							
CY7C466A-JC	ALPHA-X	4723663	219709366	128	36	0	
CY7C466A-JC	ALPHA-X	4723663	219709366	128	58	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST (150C, 5.75V)							
CY7C466A-JC	ALPHA-X	4723663	219709366	80	160	0	
CY7C466A-JC	ALPHA-X	4723663	219709366	168	160	0	
CY7C466A-JC	ALPHA-X	4723697	219710431	80	160	0	
CY7C466A-JC	ALPHA-X	4723697	219710431	168	160	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (150C, 5.75V)							
CY7C466A-JC	ALPHA-X	4723663	219709366	80	400	0	
CY7C466A-JC	ALPHA-X	4723663	219709366	500	400	0	
CY7C466A-JC	ALPHA-X	4723697	219710431	80	400	0	
CY7C466A-JC	ALPHA-X	4723697	219710431	500	400	0	
STRESS: READ & RECORD LIFE TEST (150C, 5.75V)							
CY7C466A-JC	ALPHA-X	4723663	219709366	80	10	0	
CY7C466A-JC	ALPHA-X	4723663	219709366	500	10	0	
STRESS: TC COND. C, -65 TO 150C, PRECOND. 192 HRS 30C/60%RH							
CY7C466A-JC	ALPHA-X	4723663	219709366	300	94	0	
CY7C466A-JC	ALPHA-X	4723663	219709366	1000	94	0	
CY7C466A-JC	ALPHA-X	4723697	219710431	300	90	0	
CY7C466A-JC	ALPHA-X	4723697	219710431	1000	90	0	