Cypress Semiconductor
Qualification Report

QTP# 97211, VERSION 2.0
July, 2003

1 Meg SRAM, R42D Technology, Fab 4 Qualification	
CY7C1021V33	64K x 16 Static RAM

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

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PRODUCT/TECHNOLOGY/FAB DESCRIPTION

PRODUCT DESCRIPTION (for qualification)			
Information provided in this document is intended for generic qualification and technically describes the Cypress part supplied:			
Marketing Part #:	CY7C1021V33		
Package:	44-pin, 400 mil SOJ		
Device Description:	1 Meg SRAM, R42D Technology		
Cypress Division:	Cypress Semiconductor Corporation - MPD Division		
Overall Die (or Mask) REV Level (pre-requisite for qualification):		Rev. C	
What ID markings on Die:	7C1321C		

TECHNOLOGY/FAB PROCESS DESCRIPTION - R42D			
Number of Metal Layers:	2	Metal Composition:	Metal 1: TiW,AlCu,TiW/500Å,6000Å,300Å Metal 2: TiW,AlCu,TiW/500Å,8000Å,300Å
Passivation Type and Materials:	7,000 Å TEOS + 6,000 Å SiN		
Free Phosphorus contents in top glass layer(%):	N/A		
Die Coating(s), if used:	n/a		
Generic Process Technology/Design Rule (µ-drawn):	CMOS, Single Poly, Double Metal /0.35µm		
Gate Oxide Material/Thickness (MOS):	SiO_2 / 70 Å		
Name/Location of Die Fab (prime) Facility:	Cypress Semiconductor - Bloomington, MN		
Die Fab Line ID/Wafer Process ID:	Fab4/R42D		

PLASTIC PACKAGE/ASSEMBLY DESCRIPTION

Package Outline, Type, or Name:	44-pin, 400-mil SOJ		
Mold Compound Name/Manufacturer:	NITO MP-8000CHV		
Lead Frame material:	Copper		
Lead Finish, composition:	Solder Plated, 85%Sn, 15%Pb		
Die Attach Area Plating:	Silver Spot		
Die Attach Method:	Epoxy	Die Attach Material:	Ablestik 8361
Wire Bond Method:	Thermosonic	Wire Material/Size:	Gold / 1.0 mil
JESD22-A112 Moisture Sensitivity Level	Level 1		
Assembly Line ID and Process ID:	Omedata, Indonesia		

Note: Please contact a Cypress Representative for other packages availability.

RELIABILITY TESTS PERFORMED

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc = 3.8V, 150°C	P
Long Life Verification	Dynamic Operating Condition, Vcc=3.8V, 150°C	P
Read and Record Life Test	Dynamic Operating Condition, Vcc = 3.8V, 150°C	P
High Temperature Steady State Life	Static Operating Condition, Vcc = 3.63V, 150°C	P
High Temperature Storage	165°C, no bias	P
High Accelerated Saturation Test (HAST)	140°C, 85%RH, 3.63V Precondition: JESD22 Moisture Sensitivity Level 3 192 Hrs. 30°C/60%RH	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity Level 3 192 Hrs. 30°C/60%RH	P
Current Density	Cypress Spec 22-00029	P
Age Bond Pull	MIL-STD-883, Method 2011	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V MIL-STD-883, Method 3015.7	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	1,000V Cypress Spec. 25-00020	P
Static Latchup Sensitivity	8.4V In accordance with JEDEC 17. Cypress Spec. 01-00081	P
Dynamic Latchup Sensitivity	7.0V In accordance with JEDEC 17. Cypress Spec. 01-00081	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Devive Hours	# Fails	Activation Energy	Thermal AF	Failure Rate
High Temperature Operating Life[1,] Early Failure Rate	N/A	N/A	N/A	N/A	N/A
High Temperature Operating Life[2,3] Long Term Failure Rate	1,059,000DHRs	2	0.7	170	17 FIT

[1] Early Failure Rate was not performed. Production burn-in at 48 Hrs/4.3V/150°C is performed for the product.
[2] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[3] Chi-squared 60% estimations used to calculate the failure rate.

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

RELIABILITY TEST DATA

QTP #: 97211

DEVICE	ASSY-LOC	FABLOT#	ASSYLOT#	DURATION	S/S	REJ	FAIL MODE
STRESS: ESD-CHARGE DEVICE MODEL, 1000v							
CY7C1021V33-VC	TAIWN-G	4719474	619704310	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2200V							
CY7C1021V33-VC	TAIWN-G	4719474	619704310	COMP	3	0	
STRESS: HI-ACCEL SATURATION TEST (140C, 3.63V), PRECOND. 192 HRS 30C/60%RH							
CY7C1021V33-VC	TAIWN-G	4719474	619704310	128	64	0	
CY7C1021V33-VC	TAIWN-G	4719474	619704310	256	64	0	
CY7C1021V33-VC	TAIWN-G	4721588	619705012	128	96	0	
STRESS: HIGH TEMPERATURE STORAGE (165C, NO BIAS)							
CY7C1021V33-VC	TAIWN-G	4719474	619704310	336	48	0	
CY7C1021V33-VC	TAIWN-G	4719474	619704310	1000	48	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST (150C, 3.63V)							
CY7C1021V33-VC	TAIWN-G	4719474	619704310	80	160	0	
CY7C1021V33-VC	TAIWN-G	4719474	619704310	168	160	0	
CY7C1021V33-VC	TAIWN-G	4721588	619705012	80	160	0	
CY7C1021V33-VC	TAIWN-G	4721588	619705012	168	160	0	
CY7C1021V33-VC	TAIWN-G	4722642	619705819	80	156	0	
CY7C1021V33-VC	TAIWN-G	4722642	619705819	168	156	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (150C, 3.80V)							
CY7C1021V33-VC	TAIWN-G	4719474	619704310	80	538	0	
CY7C1021V33-VC	TAIWN-G	4719474	619704310	500	538	1	1 SINGLE BIT
CY7C1021V33-VC	TAIWN-G	4721588	619705012	80	528	0	
CY7C1021V33-VC	TAIWN-G	4721588	619705012	500	528	1	1 SINGLE BIT
CY7C1021V33-VC	TAIWN-G	4722642	619705819	80	525	0	
CY7C1021V33-VC	TAIWN-G	4722642	619705819	500	525	0	
STRESS: LONG LIFE VERIFICATION (150C, 3.80V)							
CY7C1021V33-VC	TAIWN-G	4719474	619704310	1000	527	0	
STRESS: READ & RECORD LIFE TEST (150C, 3.80)							
CY7C1021V33-VC	TAIWN-G	4719474	619704310	80	10	0	
CY7C1021V33-VC	TAIWN-G	4719474	619704310	500	10	0	
STRESS: TC COND. C, -65 TO 150C, PRECOND. 192 HRS 30C/60%RH							
CY7C1021V33-VC	TAIWN-G	4719474	619704310	300	90	0	
CY7C1021V33-VC	TAIWN-G	4719474	619704310	1000	90	0	
CY7C1021V33-VC	TAIWN-G	4721588	619705012	300	96	0	
CY7C1021V33-VC	TAIWN-G	4721588	619705012	1000	96	0	
CY7C1021V33-VC	TAIWN-G	4722642	619705819	300	90	0	