Cypress Semiconductor
Qualification Report

QTP# 97201 VERSION 2.0
February, 1998

1 Meg SRAM, R32D Technology, Fab 4 Qualification	
CY7C109/CY7C1009	128K x 8 SRAM (5V Operation)
CY7C109V33/CY7C1009V33	128K x 8 SRAM (3.3V Operation)

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

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PRODUCT DESCRIPTION (for qualification)		
Information provided in this document is intended for generic qualification and technically describes the Cypress part supplied:		
Marketing Part #:	CY7C109/CY7C1009/CY7C109V33/CY7C1009V33	
Package:	32-pin, 400-mil SOJ	
Device Description:	128K x 8 Static RAM, R32D Technology	
Cypress Division:	Cypress Semiconductor Corporation	
Overall Die (or Mask) REV Level (pre-requisite for qualification):		Rev. G
What ID markings on Die:	7C109A/7C1309A	

TECHNOLOGY/FAB PROCESS DESCRIPTION - R32			
Number of Metal Layers:	2	Metal Composition:	Metal 1: Al-Cu/TiW Metal 2: TiW/Al-Cu/TiW
Passivation Type and Materials:	Silicon Dioxide 7,000Å + Silicon Nitride 6,000Å		
Number of Transitors in device	6,489,591		
Number of Gates in devices	1,622,397		
Free Phosphorus contents in top glass layer(%):	0%		
Die Coating(s), if used:	N/A		
Generic Process Technology/Design Rule (µ-drawn):	CMOS, Single Local Interconnect, Double Metal /0.5 µm		
Gate Oxide Material/Thickness (MOS):	SiO_2 / 145Å		
Name/Location of Die Fab (prime) Facility:	Cypress Semiconductor - Bloomington, MN		
Die Fab Line ID/Wafer Process ID:	Fab4/R32D		

PLASTIC PACKAGE/ASSEMBLY DESCRIPTION			
Package Outline, Type, or Name:	32-pin, 400-mil SOJ		
Mold Compound Name/Manufacturer:	Hitachi-CEL9200		
Lead Frame material:	Copper Alloy 194		
Lead Finish, composition:	Solder Plated, 90%Sn, 10%Pb		
Die Attach Area Plating:	Silver Spot		
Die Attach Method:	Epoxy	Die Attach Material:	Ablestik 8361
Wire Bond Method:	Thermosonic	Wire Material/Size:	Gold / 1.3 mil
JESD22-A112 Moisture Sensitivity Level:	Level 3		
Name/Location of Assembly (prime) facility:	Omedata, Indonesia (INDNS-O)		

Note: Please contact a Cypress Representative for other packages availability.

RELIABILITY TESTS PERFORMED

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc = 5.75V, 150°C	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc = 5.75V, 150°C	P
Read and Record Life Test	Dynamic Operating Condition, Vcc = 5.75V, 150°C	P
High Temperature Steady State Life	Static Operating Condition, Vcc = 5.750V, 150°C	P
High Accelerated Saturation Test (HAST)	140°C, 85%RH, 5.5V Precondition: JESD22 Moisture Sensitivity Level 1 (168 Hrs, 85C/85%RH) * Shipped at Level 3	P*
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity Level 1 (168 Hrs, 85C/85%RH) * Shipped at Level 3	P*
High Temp Storage	165°C, no bias	P
Electrostatic Discharge Human Body Model (ESD-HBM)	MIL-STD-883, Method 3015.7	2,200V
Electrostatic Discharge Charge Device Model (ESD-CDM)	Cypress Spec. 25-00020	2,000V
Latchup Sensitivity CY7C109/CY7C1009 CY7C109V33/CY7C1009V33	In accordance with JEDEC 17. Cypress Spec. 01-00081	 11.9V 10.0V
Current Density	Cypress Spec 22-00029	P
Age Bond Strength	MIL-STD-883, Method 2011	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[4]	Failure Rate
High Temperature Operating Life Early Failure Rate	538 Devices	0	N/A	N/A	0 PPM
High Temperature Operating Life[1,2] Long Term Failure Rate	267,500 DHRs	0	0.7	170	20 FIT

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate.
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A = The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

RELIABILITY TEST DATA

QTP#: 97201

DEVICE	ASSY-LOC	FABLOT#	ASSYLOT#	DURATION	S/S	REJ	FAIL MODE
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (150C, 5.75V)							
CY7C109-VC	INDNS-O	4726848	519708433	48	538	0	1 EOS
STRESS: ESD-CHARGE DEVICE MODEL (2000V)							
CY7C109V33-VC	INDNS-O	4725810	519708192	COMP	3	0	
CY7C109-VC	INDNS-O	4726848	519708433	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015 (2200V)							
CY7C109V33-VC	INDNS-O	4725810	519708192	COMP	3	0	
CY7C109V33-VC	INDNS-O	4725810	519709182	COMP	3	0	
CY7C109-VC	INDNS-O	4726848	519708433	COMP	3	0	
STRESS: HI-ACCEL SATURATION TEST (140C, 5.5V), PRECOND. 168 HRS 85C/85%RH							
CY7C109-VC	INDNS-O	4726848	519708433	128	45	0	1 EOS
STRESS: HIGH TEMPERATURE STORAGE (165C, NO BIAS)							
CY7C109-VC	INDNS-O	4726848	519708433	336	46	0	
CY7C109-VC	INDNS-O	4726848	519708433	500	46	0	
CY7C109-VC	INDNS-O	4726848	519708433	1000	46	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST (150C, 5.75V)							
CY7C109-VC	INDNS-O	4726848	519708433	80	78	0	
CY7C109-VC	INDNS-O	4726848	519708433	168	78	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (150C, 5.75V)							
CY7C109-VC	INDNS-O	4726848	519708433	80	535	0	2 EOS
CY7C109-VC	INDNS-O	4726848	519708433	500	535	0	
STRESS: READ & RECORD LIFE TEST (150C, 5.75V)							
CY7C109-VC	INDNS-O	4726848	519708433	80	10	0	
CY7C109-VC	INDNS-O	4726848	519708433	500	9	0	
STRESS: TC COND. C, -65 TO 150C, PRECOND. 168 HRS 85C/85%RH							
CY7C109-VC	INDNS-O	4726848	519708433	300	46	0	
CY7C109-VC	INDNS-O	4726848	519708433	1000	46	0	

DEVICE RELATED RELIABILITY TEST DATA

QTP#: 97118[1]

DEVICE	ASSY-LOC	FABLOT#	ASSYLOT#	DURATION	S/S	REJ	FAIL MODE
STRESS: ESD-CHARGE DEVICE MODEL (2,000V)							
CY7C1049-VC	SEOL-L	4714185	619702877/8	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015 (2,200V)							
CY7C1049-VC	SEOL-L	4714185	619702877/8	COMP	3	0	
STRESS: HI-ACCEL SATURATION TEST (140C, 5.5V), PRECOND. 192 HRS 30C/60%RH							
CY7C1049-VC	SEOL-L	4714215	619702951	128	45	0	
CY7C1049-VC	SEOL-L	4714215	619702951	256	44	0	
CY7C1048-SC	TAIWN-G	4716305	619703660	128	48	0	
STRESS: HIGH TEMPERATURE STORAGE (165C, NO BIAS)							
CY7C1049-VC	SEOL-L	4714215	619702951	336	46	0	
CY7C1049-VC	SEOL-L	4714215	619702951	1000	46	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST (150C, 5.75V)							
CY7C1049-VC	SEOL-L	4714215	619702951	80	76	0	
CY7C1049-VC	SEOL-L	4714215	619702951	168	76	0	
CY7C1048-SC	TAIWN-G	4716305	619703660	80	76	0	
CY7C1048-SC	TAIWN-G	4716305	619703660	168	76	0	
CY7C1048-SC	TAIWN-G	4716305	619703660	256	76	0	
CY7C1049-VC	SEOL-L	4716328	619704042	80	73	0	
CY7C1049-VC	SEOL-L	4716328	619704042	168	77	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (150C, 5.75V)							
CY7C1049-VC	SEOL-L	4714215	619702951	80	115	0	
CY7C1049-VC	SEOL-L	4714215	619702951	500	113	2	2 EOS
CY7C1048-SC	TAIWN-G	4716305	619703660	80	116	0	
CY7C1048-SC	TAIWN-G	4716305	619703660	500	116	1	1 NON VISUAL SINGLE BIT
CY7C1049-VC	SEOL-L	4716328	619704042	80	118	0	
CY7C1049-VC	SEOL-L	4716328	619704042	500	117	0	
STRESS: EXTENDED DYNAMIC BURN-IN (150C, 5.75V)							
CY7C1049-VC	SEOL-L	4714215	619702951	1000	111	0	
STRESS: COLD LIFE TEST (-30C, 6.5V)							
CY7C1049-VC	SEOL-L	4714185	619702877/8	500	45	0	
STRESS: READ & RECORD LIFE TEST (150C, 5.75V)							
CY7C1049-VC	SEOL-L	4714215	619702951	500	10	0	

[1] QTP 97118, 512K x 8 SRAM, R32D Technology, Fab 4 qualification

DEVICE RELATED RELIABILITY TEST DATA

QTP#: 97118[2]

DEVICE	ASSY-LOC	FABLOT#	ASSYLOT#	DURATION	S/S	REJ	FAIL MODE
STRESS: TC COND. C, -65 TO 150C, PRECOND. 192 HRS 30C/60%RH							
CY7C1049-VC	SEOL-L	4714185	619702877/8	300	45	0	
CY7C1049-VC	SEOL-L	4714215	619702951	300	46	0	
CY7C1049-VC	SEOL-L	4714215	619702951	1000	46	0	
CY7C1048-SC	TAIWN-G	4714185	619702975	300	45	0	
CY7C1048-SC	TAIWN-G	4714185	619702975	1000	45	0	
CY7C1049-VC	SEOL-L	4716328	619704042	300	45	0	
CY7C1049-VC	SEOL-L	4716328	619704042	1000	45	0	

[2] QTP 97118, 512K x 8 SRAM, R32D Technology, Fab 4 qualification