Cypress Semiconductor
Qualification Report

QTP# 97153, VERSION 2.0
July, 2003

64K x 18 Synchronous Cache RAM

CY7C1031/CY7C1032

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

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PRODUCT/TECHNOLOGY/FAB DESCRIPTION

PRODUCT DESCRIPTION (for qualification)			
Information provided in this document is intended for generic qualification and technically describes the Cypress part supplied:			
Marketing Part #:	CY7C1031/1032		
Package:	52-pins PLCC		
Device Description:	64K x 18 Synchronous Cache RAM		
Cypress Division:	Cypress Semiconductor Corporation - MPD Division		
Overall Die (or Mask) REV Level (pre-requisite for qualification):		Rev. E	
What ID markings on Die:	7C1031A/7C1032A		

TECHNOLOGY/FAB PROCESS DESCRIPTION - R3			
Number of Metal Layers:	2	Metal Composition:	Metal 1: 500Å TiW, 6,000Å Al/0.5%Cu 1,200Å TiW Metal 2: 500Å TiW, 9,000Å Al/0.5%Cu 1,200Å TiW
Passivation Type and Materials:	7,000A TEOS + 6,000A Si_2N_4		
Free Phosphorus contents in top glass layer(%):	0%		
Die Coating(s), if used:	n/a		
Number of Transistors in device:	7,000,000		
Number of Gates in device:	2,500,000		
Generic Process Technology/Design Rule (µ-drawn):	CMOS, Single Poly, Double Metal /0.5 µm		
Gate Oxide Material/Thickness (MOS):	SiO_2 / 145 Å		
Name/Location of Die Fab (prime) Facility:	Cypress Semiconductor - Bloomington, MN		
Die Fab Line ID/Wafer Process ID:	Fab4/R3		

PLASTIC PACKAGE/ASSEMBLY DESCRIPTION

Package Outline, Type, or Name:	52-Lead PLCC		
Mold Compound Name/Manufacturer:	Nitto-8000		
Lead Frame material:	Copper		
Die Coatings (if used):	None		
Lead Finish, composition:	Solder Plated, 85%Sn, 15%Pb		
Die Attach Area Plating:	Silver Spot		
Die Attach Method:	Paste	Die Attach Material:	Silver Epoxy
Wire Bond Method:	Thermosonic	Wire Material/Size:	Gold / 1.3 mil
JESD22-A12 Moisture Sensitivity Level	Level 3		
Name/Location of Assembly (prime) facility:	Omedata, Inonesia (INDNS-O)		

Note: Please contact a Cypress Representative for other packages availability.

RELIABILITY TESTS PERFORMED

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc = 5.75V, 150°C	P
Read and Record Life Test	Dynamic Operating Condition, Vcc = 5.75V, 150°C	P
High Temperature Steady State Life	Static Operating Condition, Vcc = 5.75V, 150°C	P
High Accelerated Saturation Test (HAST)	140°C, 85%RH, 5.5V Precondition: JESD22 Moisture Sensitivity Level 3 192 Hrs. 30°C/60%RH	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity Level 1 168 Hrs. 85°C/85%RH	P
Acoustic Microscopy	Cypress Spec 25-000104	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V MIL-STD-883, Method 3015.7	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V Cypress Spec. 25-00020	P
Latchup Sensitivity	12V In accordance with JEDEC 17. Cypress Spec. 01-00081	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Devive Hours	# Fails	Activation Energy	Thermal AF[4]	Failure Rate
High Temperature Operating Life[1,] Early Failure Rate	N/A	N/A	N/A	N/A	N/A
High Temperature Operating Life[2,3] Long Term Failure Rate	395,143DHRs	1	0.6	170	15 FIT

[1] Early Failure Rate was not performed. Production burn-in at 80 Hrs/6.5V/150°C °C is performed for the product.
[2] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[3] Chi-squared 60% estimations used to calculate the failure rate. Failure Rate was calculated for CY7C1031, R3 technology, Fab 4 qualification (QTP 97153, 96344 and 96491).
[4] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

RELIABILITY TEST DATA

QTP#: 97153[1]

DEVICE	ASSY-LOC	FABLOT#	ASSYLOT#	DURATION	S/S	REJ	FAIL MODE
STRESS: HI-ACCEL SATURATION TEST (140C, 5.5V), PRECOND. 192 HRS 30C/60%RH							
7C1031EC-OJCB	INDNS-O	4705764	519704270	128	45	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST (150C, 5.75V)							
7C1031EC-OJCB	INDNS-O	4702633	519703880	80	80	0	
7C1031EC-OJCB	INDNS-O	4702633	519703880	168	80	0	
7C1031EC-OJCB	INDNS-O	4705764	519704270	80	152	1	1 PARTICLE
7C1031EC-OJCB	INDNS-O	4705764	519704270	168	151	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (150C, 5.75V)							
7C1031EC-OJCB	INDNS-O	4702633	519703880	80	120	0	
7C1031EC-OJCB	INDNS-O	4702633	519703880	500	116	1	1 BAKE SENSITIVE/NON VISUAL
7C1031EC-OJCB	INDNS-O	4705764	519704270	80	117	0	
7C1031EC-OJCB	INDNS-O	4705764	519704270	500	107	0	
STRESS: READ & RECORD LIFE TEST (150C, 5.75V)							
7C1031EC-OJCB	INDNS-O	4702633	519703880	48	10	0	
7C1031EC-OJCB	INDNS-O	4702633	519703880	500	10	0	
STRESS: TC COND. C, -65 TO 150C, PRECOND. 168 HRS 85C/85%RH							
7C1031EC-OJCB	INDNS-O	4704720	519703879	300	48	0	
7C1031EC-OJCB	INDNS-O	4702633	519703880	300	50	0	
7C1031EC-OJCB	INDNS-O	4702633	519703880	1000	50	0	
7C1031EC-OJCB	INDNS-O	4705764	519704270	300	47	0	

[1] QTP 97153, CY7C1031 (Rev. E), R3 Technology, Fab 4 qualification. Memory cell is changed to the “Double ladder cell” (no gap mask for poly) to improve A/C latch up performance.

DEVICE RELATED RELIABILITY TEST DATA

QTP#: 96344[2]

DEVICE	ASSY-LOC	FABLOT#	ASSYLOT#	DURATION	S/S	REJ	FAIL MODE
STRESS: HI-ACCEL SATURATION TEST (140C, 5.5V), PRECOND. DB + 72 HRS 30C/60%RH							
CY7C1031-JC	INDNS-O	4612138	519607961	128	64	0	
CY7C1031-JC	INDNS-O	4613186	519608290	128	48	0	
STRESS: HIGH TEMPERATURE STORAGE (165C, NO BIAS)							
CY7C1031-JC	INDNS-O	4612138	519607961	336	79	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST (150C, 5.75V)							
CY7C1031-JC	INDNS-O	4615243	519608948	80	121	0	
CY7C1031-JC	INDNS-O	4615243	519608948	168	105	0	
CY7C1031-JC	INDNS-O	4616282	519608949	80	131	0	
CY7C1031-JC	INDNS-O	4616282	519608949	168	126	0	
CY7C1031-JC	INDNS-O	4618372	519609647	80	126	0	
CY7C1031-JC	INDNS-O	4618372	519609647	168	126	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (150C, 5.75V)							
CY7C1031-JC	INDNS-O	4615243	519608948	80	195	0	
CY7C1031-JC	INDNS-O	4615243	519608948	317	190	0	
CY7C1031-JC	INDNS-O	4615243	519608948	500	179	0	
CY7C1031-JC	INDNS-O	4616282	519608949	80	195	0	
CY7C1031-JC	INDNS-O	4616282	519608949	317	195	0	
CY7C1031-JC	INDNS-O	4616282	519608949	500	187	0	
CY7C1031-JC	INDNS-O	4618372	519609647	80	195	0	
CY7C1031-JC	INDNS-O	4618372	519609647	300	185	0	
CY7C1031-JC	INDNS-O	4618372	519609647	500	184	0	
STRESS: COLD LIFE TEST (-45C, 6.5V)							
CY7C1031-JC	INDNS-O	4601761	519602525	500	47	0	
CY7C1031-JC	INDNS-O	4601761	519602525	1000	47	0	
STRESS: TC COND. C, -65 TO 150C, PRECOND. DBAKE + 72 HRS 30/60%RH							
CY7C1031-JC	INDNS-O	4612138	519607961	300	79	0	
CY7C1031-JC	INDNS-O	4613173	519608123	300	79	0	
CY7C1031-JC	INDNS-O	4613186	519608290	300	79	0	

[2] QTP 96344, CY7C1031 (Rev. B), R30 Technology qualified in Fab 4.

DEVICE RELATED RELIABILITY TEST DATA

QTP#: 96491[3]

DEVICE	ASSY-LOC	FABLOT#	ASSYLOT#	DURATION	S/S	REJ	FAIL MODE
STRESS: HI-ACCEL SATURATION TEST (140C, 5.5V), PRECOND. 192 HRS 30C/60%RH							
CY7C1031-JC	INDNS-O	4621458	519611316	128	63	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST (150C, 5.75V)							
CY7C1031-JC	INDNS-O	4621458	519609977	80	129	0	
CY7C1031-JC	INDNS-O	4621458	519609977	168	128	0	
STRESS: READ & RECORD LIFE TEST (150C, 5.75V)							
CY7C1031-JC	INDNS-O	4621458	519609977	80	11	0	
CY7C1031-JC	INDNS-O	4621458	519609977	500	11	0	
STRESS: TC COND. C, -65 TO 150C, PRECOND. 192 HRS 30C/60%RH							
CY7C1031-JC	INDNS-O	4621458	519609977	300	42	0	
CY7C1031-JC	INDNS-O	4621458	519609977	300	78	0	
CY7C1031-JC	INDNS-O	4621458	519609977	1000	41	0	

[3] QTP 96491, CY7C1031 (Rev. D), R30 Technology, Fab 4 Qualification redesigned with all layer masks changed. Moisture Sensitivity Level was upgraded from level 5 to level 3 (ship with dry-baked/dry-packed).