Cypress Semiconductor
Qualification Report

QTP# 97101 VERSION 2.0
July, 2003

64K x 16 Static RAM
CY7C1021

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

Ed Russell
Reliability Director
(408) 432–7069

Rene Rodgers
Reliability Engineering
(408) 943-2732

PRODUCT DESCRIPTION (for qualification)			
Information provided in this document is intended for generic qualification and technically describes the Cypress part supplied:			
Marketing Part #:	CY7C1021		
Package:	44 pins, 400 mil SOJ		
Device Description:	64K x 16 Static RAM		
Cypress Division:	Cypress Semiconductor Corporation - MPD Division		
Overall Die (or Mask) REV Level (pre-requisite for qualification):		Rev. B	
What ID markings on Die:	7C1021A		

TECHNOLOGY/FAB PROCESS DESCRIPTION - R3			
Number of Metal Layers:	2	Metal Composition:	Metal 1: 500A TiW, 6000A Al/0.5%Cu 1200A TiW Metal 2: 500A TiW, 9000A Al/0.5%Cu 1200A TiW
Passivation Type and Materials:	7,000A TEOS + 6,000A Si_2N_4		
Free Phosphorus contents in top glass layer(%):	0%		
Die Coating(s), if used:	None		
Number of Transitor in device	6,507,935		
Number of Gate in device	6,565,448		
Generic Process Technology/Design Rule (µ-drawn):	CMOS, Single Poly, 2 Local Interconnect, Double Metal /0.5 µm		
Gate Oxide Material/Thickness (MOS):	SiO_2 / 145Å		
Name/Location of Die Fab (prime) Facility:	Cypress Semiconductor - Bloomington, MN		
Die Fab Line ID/Wafer Process ID:	Fab4/R3		

PLASTIC PACKAGE/ASSEMBLY DESCRIPTION			
Package Outline, Type, or Name:	44-pin, 400 mil SOJ		
Mold Compound Name/Manufacturer:	Nito-MP8000		
Lead Frame material:	A194 FH		
Lead Finish, composition:	Solder Plated, 85%Sn, 15%Pb		
Die Attach Area Plating:	Silver Spot		
Die Attach Method:	Paste	Die Attach Material:	Ablestik 8361A
Wire Bond Method:	Thermosonic	Wire Material/Size:	Gold / 1.0 mil
JESD22-A112 Moisture Sensitivity Level	Level 3		
Assembly Line ID and Process ID:	ASE, Taiwan (TAIWN-G)		

Note: Please contact a Cypress Representative for other packages availability.

RELIABILITY TESTS PERFORMED

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc = 5.75V, 150°C	P
Read and Record Life Test	Dynamic Operating Condition, Vcc = 5.75V, 150°C	P
High Temperature Steady State Life	Static Operating Condition, Vcc = 5.75V, 150°C	P
High Accelerated Saturation Test (HAST)	140°C, 85%RH, 5.5V Precondition: JESD22 Moisture Sensitivity Level 3 (192 Hrs, 30C/60% RH)	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity Level 3 (192 Hrs, 30C/60% RH)	P
Electrostatic Discharge Human Body Model (ESD-HBM)	1800V MIL-STD-883, Method 3015.7	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V Cypress Spec. 25-00020	P
Latchup Sensitivity	12V In accordance with JEDEC 17. Cypress Spec. 01-00081	P
Dynamic Latchup sensitivity	7.1V Cypress Spec. 01-00081	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF	Failure Rate
High Temperature Operating Life Early Failure Rate[2]	N/A	N/A	N/A	N/A	N/A
High Temperature Operating Life[1,3] Long Term Failure Rate	59,000 DHRs	0	0.7	170	** FIT

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Production burn-in @ 80 Hrs/150°C/6.5V is performed for this device.
[3] Chi-squared 60% estimations used to calculate the failure rate.

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

** Sample size insufficient for accurate FIT Rate calculation.

RELIABILITY TEST DATA

QTP#: 97101

DEVICE	ASSY-LOC	FABLOT#	ASSYLOT#	DURATION	S/S	REJ	FAIL MODE
STRESS: ESD-CHARGE DEVICE MODEL (500V)							
CY7C1021-VC	TAIWN-G	4711049	619703241	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015 (1800V)							
CY7C1021-VC	TAIWN-G	4711049	619703241	COMP	3	0	
CY7C1021-VC	TAIWN-G	4711049	619703241	COMP	3	0	
STRESS: HI-ACCEL SATURATION TEST (140C, 5.5V), PRECOND. 192 HRS 30C/60%RH							
CY7C1021-VC	TAIWN-G	4711049	619703241	128	48	1	1 LIFTING BOND
CY7C1021-VC	TAIWN-G	4711049	619703241L1	128	48	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST (150C, 5.75V)							
CY7C1021-VC	TAIWN-G	4711049	619703241	76	75	0	
CY7C1021-VC	TAIWN-G	4711049	619703241	168	75	0	
CY7C1021-VC	TAIWN-G	4711049	619703241	80	76	0	
CY7C1021-VC	TAIWN-G	4711049	619703241	168	76	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (150C, 5.75V)							
CY7C1021-VC	TAIWN-G	4711049	619703241	80	118	0	
CY7C1021-VC	TAIWN-G	4711049	619703241	500	118	0	
STRESS: READ & RECORD LIFE TEST (150C, 5.75V)							
CY7C1021-VC	TAIWN-G	4711049	619703241	500	10	0	
STRESS: TC COND. C, -65 TO 150C, PRECOND. 192 HRS 30C/60%RH							
CY7C1021-VC	TAIWN-G	4711049	619703241	300	48	0	
CY7C1021-VC	TAIWN-G	4711049	619703241	1000	48	0	