Cypress Semiconductor
Qualification Report

QTP# 97044, VERSION 1.1
November, 2002

32K x 16 SRAM, R3 Technology, Fab 4 Qualification	
CY7C1020	32K x 16, 5V Static RAM
CY7C1020V33	32K x 16, 3.3V Static RAM

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

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PRODUCT/TECHNOLOGY/FAB DESCRIPTION

PRODUCT DESCRIPTION (for qualification)	
Information provided in this document is intended for generic qualification and technically describes the Cypress part supplied:	
Marketing Part #:	CY7C1020/CY7C1020V33
Package:	44-pin, 400 mil SOJ
Device Description:	32K x 16 SRAM, R3 Technology
Cypress Division:	Cypress Semiconductor Corporation - MPD Division
Overall Die (or Mask) REV Level (pre-requisite for qualification):	Rev. A
What ID markings on Die:	7C1020A

TECHNOLOGY/FAB PROCESS DESCRIPTION - R3			
Number of Metal Layers:	2	Metal Composition:	Metal 1: 500Å TiW, 6,000Å Al/0.5%Cu 1,200Å TiW Metal 2: 500Å TiW, 9,000Å Al/0.5%Cu 1,200Å TiW
Passivation Type and Materials:	7,000A TEOS + 6,000A Si_2N_4		
Free Phosphorus contents in top glass layer(%):	0%		
Die Coating(s), if used:	n/a		
Number of Transistors in device:	3,243,096		
Number of Gates in device:	32,456		
Generic Process Technology/Design Rule (µ-drawn):	CMOS, Single Poly, Double Metal /0.5 µm		
Gate Oxide Material/Thickness (MOS):	SiO_2 / 145 Å		
Name/Location of Die Fab (prime) Facility:	Cypress Semiconductor - Bloomington, MN		
Die Fab Line ID/Wafer Process ID:	Fab4/R3		

PLASTIC PACKAGE/ASSEMBLY DESCRIPTION

Package Outline, Type, or Name:	44-pin, 400-mil SOJ		
Mold Compound Name/Manufacturer:	Sumitomo EME-6300		
Lead Frame material:	Copper		
Lead Finish, composition:	Solder Plated, 85%Sn, 15%Pb		
Die Attach Area Plating:	Silver Spot		
Die Attach Method:	Epoxy	Die Attach Material:	Ablestik 84-1MISR4
Wire Bond Method:	Thermosonic	Wire Material/Size:	Gold / 1.3 mil
JESD22-A112 Moisture Sensitivity Level	Level 3		
Assembly Line ID and Process ID:	ASE, Taiwan (Taiwn-G)		

Note: Please contact a Cypress Representative for other packages availability.

RELIABILITY TESTS PERFORMED

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc = 5.75V, 150°C	P
Read and Record Life Test	Dynamic Operating Condition, Vcc = 5.75V, 150°C	P
High Temperature Steady State Life	Static Operating Condition, Vcc = 5.75V, 150°C	P
High Accelerated Saturation Test (HAST)	140°C, 85%RH, 5.5V Precondition: JESD22 Moisture Sensitivity Level 3 192 Hrs. 30°C/60%RH	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity Level 3 192 Hrs. 30°C/60%RH	P
Electrostatic Discharge Human Body Model (ESD-HBM)	MIL-STD-883, Method 3015.7	1,600V
Electrostatic Discharge Charge Device Model (ESD-CDM)	Cypress Spec. 25-00020	750V
Latchup Sensitivity	In accordance with JEDEC 17. Cypress Spec. 01-00081	12V (CY7C1020) 11V (CY7C1020V33)

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Devive Hours	# Fails	Activation Energy	Thermal AF[4]	Failure Rate
High Temperature Operating Life[1,] Early Failure Rate	N/A	N/A	N/A	N/A	N/A
High Temperature Operating Life[2,3] Long Term Failure Rate	59,000DHRs	0	0.7	170	91 FIT

[1] Early Failure Rate was not performed. Production burn-in at 80 Hrs/6.5V/150°C °C is performed for the product.
[2] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[3] Chi-squared 60% estimations used to calculate the failure rate.
[4] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A = The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

RELIABILITY TEST DATA

QTP#: 97044

DEVICE	ASSY-LOC	FABLOT#	ASSYLOT#	DURATION	S/S	REJ	FAIL MODE
STRESS: ESD-CHARGE DEVICE MODEL, 750V							
CY7C1020-VC	TAIWN-G	4704730	619701268	COMP	3	0	
7C1320AC-GVC	TAIWN-G	4704730	619702345	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 1600V							
CY7C1020-VC	TAIWN-G	4704730	619701268	COMP	3	0	
CY7C1020V33-VC	TAIWN-G	4704730	619702345	COMP	3	0	
STRESS: HI-ACCEL SATURATION TEST (140C, 5.5V), PRECOND. 192 HRS 30C/60%RH							
CY7C1020-VC	TAIWN-G	4704730	619701268	128	48	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST (150C, 5.75V)							
CY7C1020-VC	TAIWN-G	4704730	619701268	80	78	0	
CY7C1020-VC	TAIWN-G	4704730	619701268	168	78	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (150C, 5.75V)							
CY7C1020-VC	TAIWN-G	4704730	619701268	80	118	0	
CY7C1020-VC	TAIWN-G	4704730	619701268	500	118	0	
STRESS: READ & RECORD LIFE TEST (150C, 5.75V)							
CY7C1020-VC	TAIWN-G	4704730	619701268	48	10	0	
CY7C1020-VC	TAIWN-G	4704730	619701268	500	10	0	
STRESS: TC COND. C, -65 TO 150C, PRECOND. 192 HRS 30C/60%RH							
CY7C1020-VC	TAIWN-G	4704730	619701268	300	48	0	