Cypress Semiconductor
Qualification Report

QTP# 96494, VERSION 1.0
August, 1997

FCT 16-Bit Family, 3.3V, R3 Technology, Fab 4 Qualification

CY74FCT163*/CY74FCT163H*

PRODUCT/TECHNOLOGY/FAB DESCRIPTION

PRODUCT DESCRIPTION (for qualification)			
Information provided in this document is intended for generic qualification and technically describes the Cypress part supplied: All CY74FCT163* and CY74FCT163H* in commercial, plastic package.			
Marketing Part #:	CY74FCT163952TPVC		
Package:	56-pin SSOP		
Device Description:	FCT 16-Bit, 3.3V, R3 Technology		
Cypress Division:	Cypress Semiconductor Corporation - CPD Division		
Overall Die (or Mask) REV Level (pre-requisite for qualification):		Rev. A	
Die Size (stepping):	59 mils x 89 mils	What ID markings on Die:	7C73580A/7C73680A

TECHNOLOGY/FAB PROCESS DESCRIPTION - R3			
Number of Metal Layers:	2	Metal Composition:	Metal 1: 500Å TiW, 6,000Å Al/0.5%Cu 1,200Å TiW Metal 2: 500Å TiW, 9,000Å Al/0.5%Cu 1,200Å TiW
Passivation Type and Materials:	7,000A TEOS + 6,000A Si_2N_4		
Free Phosphorus contents in top glass layer (%):	4-5%		
Die Coating(s), if used:	n/a		
Number of Transistors in device:	11,264		
Number of Gates in device:	2,816		
Generic Process Technology/Design Rule (µ-drawn):	CMOS, Single Poly, Double Metal /0.5 µm		
Gate Oxide Material/Thickness (MOS):	SiO_2 / 145 Å		
Name/Location of Die Fab (prime) Facility:	Cypress Semiconductor - Bloomington, MN		
Die Fab Line ID/Wafer Process ID:	Fab4/R3		

PLASTIC PACKAGE/ASSEMBLY DESCRIPTION

Package Outline, Type, or Name:	56-pin SSOP		
Mold Compound Name/Manufacturer:	Sumitomo EME-6300		
Lead Frame material:	Copper		
Lead Finish, composition:	Solder Plated, 85%Sn, 15%Pb		
Die Attach Area Plating:	Silver Spot		
Die Attach Method:	Epoxy	Die Attach Material:	Ablestik 84-1MISR4
Wire Bond Method:	Thermosonic	Wire Material/Size:	Gold / 1.3 mil
JESD22-A112 Moisture Sensitivity Level	Level 1		
Assembly Line ID and Process ID:	Unisem, Malaysia		

Note: Please contact a Cypress Representative for other packages availability.

RELIABILITY TESTS PERFORMED

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc = 3.6V, 150°C	P
Read and Record Life Test	Dynamic Operating Condition, Vcc = 3.6V, 150°C	P
High Temperature Steady State Life	Static Operating Condition, Vcc = 3.6V, 150°C	P
High Accelerated Saturation Test (HAST)	140°C, 85%RH, 3.6V Precondition: JESD22 Moisture Sensitivity Level 1 168 Hrs. 85°C/85%RH	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity Level 1 168 Hrs. 85°C/85%RH	P
Electrostatic Discharge Human Body Model (ESD-HBM)	MIL-STD-883, Method 3015.7	P 2,200V
Electrostatic Discharge Charge Device Model (ESD-CDM)	Cypress Spec. 25-00020	P 1,500V
Latchup Sensitivity	In accordance with JEDEC 17. Cypress Spec. 01-00081	V

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Devive Hours	# Fails	Activation Energy	Thermal AF[3]	Failure Rate
High Temperature Operating Life Early Failure Rate	762	0	N/A	N/A	0 PPM
High Temperature Operating Life[1,2] Long Term Failure Rate	64,000	0	0.7	170	84 FIT

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate.
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A = The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

RELIABILITY TEST DATA

QTP #: 96494

DEVICE	ASSY-LOC	FABLOT#	ASSYLOT#	DURATION	S/S	REJ	FAIL MODE
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (150C, 3.6V)							
CY74FCT163952TPVC	MALAY-U	4648487	349701564	48	762	0	
STRESS: ESD-CHARGE DEVICE MODEL (1,500V)							
CY74FCT163952TPVC	MALAY-U	4648487	349701564	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015 (2,200V)							
CY74FCT163952TPVC	MALAY-U	4648487	349701564	COMP	3	0	
STRESS: HI-ACCEL SATURATION TEST (140C, 3.6V), PRECOND. 168 HRS 85C/85%RH							
CY74FCT163952TPVC	MALAY-U	4648487	349701564	128	40	0	1 EOS
STRESS: HIGH TEMP STEADY STATE LIFE TEST (150C, 3.6V)							
CY74FCT163952TPVC	MALAY-U	4648487	349701564	80	78	0	
CY74FCT163952TPVC	MALAY-U	4648487	349701564	168	78	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (150C, 3.6V)							
CY74FCT163952TPVC	MALAY-U	4648487	349701564	80	128	0	
CY74FCT163952TPVC	MALAY-U	4648487	349701564	500	128	0	
STRESS: READ & RECORD LIFE TEST (150C, 3.6V)							
CY74FCT163952TPVC	MALAY-U	4648487	349701564	500	10	0	
STRESS: TC COND. C, -65 TO 150C, PRECOND. 168 HRS 85C/85%RH							
CY74FCT163952TPVC	MALAY-U	4648487	349701564	300	48	0	
CY74FCT163952TPVC	MALAY-U	4648487	349701564	1000	48	0	