Qualification Report

November, 1994 - QTP# 93101 Version 1.1

CMOS2AN PROCESS	
MARKETING PART NUMBER	DEVICE DESCRIPTION
VIC64	VMEbus Interface Controller with D64
VIC068A	VMEbus Interface Controller
VAC068A	VMEbus Address Controller
CY7C964	Bus Interface Logic Circuit

PRODUCT DESCRIPTION (for qualification)

Information provided in this document is intended for generic qualification and technically describes the Cypress part supplied: Bus Interface Products

Field	Value
Marketing Part #:	VIC64, VIC068A
Device Description:	Bus Interface Products
Cypress Division:	Cypress Semiconductor Corporation
Overall Die (or Mask) REV Level (pre-requisite for qualification):	Rev. A
Die Size (stepping):	315 mils x 312 mils
What ID markings on Die:	
Cypress Qualification completion/Marketing Availability Dates (Current REV):	November, 1994

TECHNOLOGY/FAB PROCESS DESCRIPTION - CMOS2AN

Field	Value
Number of Metal Layers:	2
Metal Composition:	Metal 1: Al, 1% Si Metal 2: Al, 1% Si
Passivation Type and Materials:	7K TEOS + 6K Nitride
Free Phosphorus contents in top glass layer(%):	None
Die Coating(s), if used:	N/A
Generic Process Technology/Design Rule (µ-drawn):	CMOS, 1.2 µm
Gate Oxide Material/Thickness (MOS):	SiO_2 / 250 A
Name/Location of Die Fab (prime) Facility:	Fab 3, Bloomington, MN
Die Fab Line ID/Wafer Process ID:	Fab3 / CMOS2AN

PLASTIC PACKAGE/ASSEMBLY DESCRIPTION			
Package Outline, Type, or Name:	144-Pin Plastic Pin Grid Array		
Die to Package edge clearance:	42 mils per side		
Mold Compound Name/Manufacturer:	Sumitomo EME-6300H(R)		
Lead Frame material:	Copper		
Lead Finish, composition:	Solder Dipped, 90%Sn, 10%Pb		
Die Attach Area Plating:	Gold	Die Attach Pad Dim:	400 mils x 400 mils
Die Attach Method:	Gold Ball	Die Attach Material:	Silver Epoxy
Wire Bond Method:	Wire	Wire Material/Size:	Gold / 1.3 mil
Name/Location of Assembly (prime) facility:	VLSI, Texas		
Assembly Line ID and Process ID:	USA-V /PPGA		

HERMETIC PACKAGE/ASSEMBLY DESCRIPTION			
Package Outline, Type, or Name:	144-Pin Ceramic Pin Grid Array		
Die to Package edge clearance:	80 mils per side		
Mold Compound Name/Manufacturer:	N/A		
Lead Frame material:	Kovar/Gold		
Lead Finish, composition:	.06 mil. Au over 0.1 mil. Nikel		
Die Attach Area Plating:	Au	Die Attach Pad Dim:	400 mils x 400 mils
Die Attach Method:	Silver Glass	Die Attach Material:	Silver Epoxy
Wire Bond Method:	Wire	Wire Material/Size:	Al-Si / 1.25 mil
Name/Location of Assembly (prime) facility:	VLSI, Texas		
Assembly Line ID and Process ID:	USA-V /CPGA		

HERMETIC PACKAGE/ASSEMBLY DESCRIPTION			
Package Outline, Type, or Name:	160 Lead Ceramic Quad Flatpack		
Die to Package edge clearance:	55 mils per side		
Mold Compound Name/Manufacturer:	N/A		
Lead Frame material:	Alloy 42		
Lead Finish, composition:	Gold Plate		
Die Attach Area Plating:	None	Die Attach Pad Dim:	425 mils x 425 mils
Die Attach Method:	Silver Glass	Die Attach Material:	Silver Epoxy
Wire Bond Method:	Ultrasonic	Wire Material/Size:	Al-Si / 1.25 mil
Name/Location of Assembly (prime) facility:	VLSI, Texas		
Assembly Line ID and Process ID:	USA-V /CQFP		

CYPRESS
SEMICONDUCTOR

OTHER INFORMATION

For approval by similarity, identify other devices using the same basic die with bonding or metal mask options or test selections and explain: All CMOS2N products: VIC068A, VAC068A, VIC64, 7C964

If Cypress is planning any changes in the near future, identify change (Qtr/Yr) in:

Die Design Rev./Shrink:		Die Process Change:	
Fab/Assembly site change:		Cross Licensee/Licensor:	
Other Devices to be qualified in this technology:			
Other Packages to be qualified for this device:	Ceramic/plastic Quad Flatpack Ceramic/Plastic Pin Grid Array		
ESD Voltage Rating (per MIL STD-008, Method 3018):	> 1,000V		
Flammability Classification (UL-94V):	None		
Alternate Fab/Assembly Locations:	Assembly :		

Please attach the following Qualification / Reliability data for the die revision and Package type, for the fab and assembly sites identified above (mark [X] if included):

1	X	HAST (5.5V, 140°C, 85%RH, 15psig)	7	X	Operating Life at (temp):	150°C/125°C
2	X	Temperature Cycles (-65°C to 150°C)	8	X	Steady State Life (HTSSL, 5.75V, 150°C)	
3		Temperature Cycles (-40°C to 165°C)	9	X	Steady State Life (HTSSL, 5.5V, 125°C)	
4		Data Retention Bake, Plastic (165°C)	10	X	Latchup Testing	
5		Data Retention Bake, Hermetic (250°C)	11	X	ESD Tests (MIL-STD 883, method 3015)	
6	X	Autoclave (PCT, 121°C, 100%RH)	12	X	Other:	Current Density Input Capacitance Internal Water Vapor Aged Bond Strength SEM Analysis Long Life Verification

PRODUCT INFORMATION FOR QUALIFICATION BY SIMILARITY

Product Family: **VMEBus CMOS2AN Process**

Mfg Division: **Cypress Semiconductor**

Supplier's Part Number		Pkg Size/ Type	Die Rev.	Die Size mil x mil (stepping)	Design Rule (μ)	Fabrication		Passivation Type	Assembly Line Location	ESD Volt Rating	Availa bility
						Process ID	Line ID				
VIC64	-BC -GC/GM/GMB -NC -UC/UM/UMB	144-Pin PPGA 144-Pin CPGA 160-Lead PQFP 160-Lead CQFP	A	315 x 312	1.2μm	CMOS2N	3	TEOS + NITRIDE	VLSI, TX	> 1,000V HBM	5/94
VIC068A	-BC -GC/GI/GM/GMB -NC -UC/UI/UM/UMB	144-Pin PPGA 144-Pin CPGA 160-Lead PQFP 160-Lead CQFP	A	315 x 312	1.2μm	CMOS2N	3	TEOS + NITRIDE	VLSI, TX	> 1,000V HBM	5/94
VAC068A	-BC -GC/GI/GM/GMB -NC -UC/UI/UM/UMB	144-Pin PPGA 144-Pin CPGA 160-Lead PQFP 160-Lead CQFP	A	315 x 312	1.2μm	CMOS2N	3	TEOS + NITRIDE	VLSI, TX	> 1,000V HBM	5/94
CY7C964	-NC -UC/UI/UM/UMB	64-Lead PQFP 64-Lead CQFP	A	148 x 145	1.2μm	CMOS2N	3	TEOS + NITRIDE	VLSI, TX	> 1,000V HBM	5/94

DEVICE RELIABILITY SUMMARY

Marketing Part:	VIC064/VIC068A	Wafer Fab:	Fab3, Bloomington, Mn
Pkg Description:	144-pins Ceramic Pin Grid Array 144-pins Plastic Pin Grid Array	Assembly:	VLSI, Texas

High Temperature Dynamic Operating Life (HTOL, 5.5V, 150°C) - Early Failure Rate					
Device	Assy Lot#	48 Hours			Cumulative
7C068D-GMB	49306887	0/337			0/337

High Temperature Dynamic Operating Life (HTOL, 5.5V, 125°C) - Early Failure Rate					
Device	Assy Lot#	96 Hours			Cumulative
7C068D-BC	49306061	0/336			0/672
7C068D-BC	49306148	0/336			

High Temperature Dynamic Operating Life (HTOL, 6.5V, 125°C) - Latent Failure Rate					
Device	Assy Lot#	168 Hours	1000 Hours		Cumulative
7C068D-BC	49306061	0/77	0/77		0/154
7C068D-BC	49306148	0/77	0/77		

High Temperature Dynamic Operating Life (HTOL, 5.5V, 150°C) - Latent Failure Rate					
Device	Assy Lot#	80 Hours	500 Hours		Cumulative
7C068D-GM	49306887	0/77	0/77		0/77

High Temperature Steady State Life Test (HTSSL, 5.75V, 150°C)					
Device	Assy Lot#	168 Hours			Cumulative
7C068D-GMB	49306887	0/78			0/78

High Temperature Steady State Life Test (HTSSL, 5.75V, 125°C)					
Device	Assy Lot#	336 Hours			Cumulative
7C068D-BC	49306148	0/78			0/156
7C068D-BC	49306061	0/78			

Long Life Verification (LLVA , 5.5V, 150C)					
Device	Assy Lot#	1000 Hours	2000 Hours		Cumulative
7C068D-GM	49306887	0/76	0/76		0/76

Group C, Subgroup1, Lifet Test (HTOL, 5.75V, 125°C)					
Device	Assy Lot#	184 Hours			Cumulative
7C064-UMB	V05032	0/80			0/80

Temperature Cycle (Condition C, -65°C to 150°C)					
Device	Assy Lot#	100 Cycles	300 Cycles	1000 Cycles	Cumulative
7C068D-BC	49306061		0/47	0/47	0/139
7C068D-BC	V11012		0/47	0/47	
7C068D-GMB	V11139	0/45		0/45	

High Accelerated Saturation Test (HAST, 5.5V, 140°C, 85%RH, 15psig)					
Device	Assy Lot#	128 Hours			Cumulative
7C068D-BC	49306061	0/45			0/90
7C068D-BC	49306148	0/45			

Pressure Cooker Test (PCT 100% RH 121°C, 15psig)					
Device	Assy Lot#	168 Hours			Cumulative
7C068D-BC	11048A	0/50			0/100
7C068D-BC	11049A	0/50			

DEVICE RELIABILITY SUMMARY

Marketing Part: VIC064/VIC068A
Wafer Fab: Fab3, Bloomington, Mn
Pkg Description: 144-pins Ceramic Pin Grid Array
144-pins Plastic Pin Grid Array
Assembly: VLSI, Texas

CMOS2AN PROCESS		
VIC64/VIC068A/VAC068A/7C964		
Electrostatic Discharge		
Human Body Model Circuit per Mil Std 883, Method 3015		
> + 1,000V	Unit 1	> -1,000V
> + 1,000V	Unit 2	> -1,000V
> + 1,000V	Unit 3	> -1,000V
(Highest passing voltage, + 10% Guard banded)		

Latchup
Testing to Cypress Internal Latch-up Procedure
3 Tests:
Current Injection = 200mA Trigger
Hot Socket = V_{CC} 0 - 8V
Temp = 125°C

Other miscellaneous tests	
Current Density	Pass
SEM Cross Section (3 wafers)	Pass
Input Capacitance	Pass
Internal Water Vapor	Pass
Aged Bond Strength	Pass
Assembly In Line	Pass