Qualification Report

February 1997, QTP# 95521 Version 2.0

Pentium™ Processor Compatible Clock Synthesizer/Driver	
Mktg Part	Description
CY2254ASC-1 CY2254ASC-2	Pentium Processor Compatible Clock Synthesizer/Driver
CY2260SC-1 CY2260SC-2 CY2260SC-3 CY2260SC-3H	Clock Synthesizer/Driver for Pentium Pro(TM) Processor
CY2252SC-1	Mobile Pentium(TM) Processor Compatible Clock Synthesizer/Driver

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PRODUCT DESCRIPTION (for qualification)			
Information provided in this document is intended for generic qualification and technically describes the Cypress part supplied:			
Marketing Part #:	CY2254ASC		
Package:	28 Pins, 300 mil SOIC		
Device Description:	Clock Synthesizer/Driver		
Cypress Division:	Cypress Semiconductor Corporation - CPD Division		
Overall Die (or Mask) REV Level (pre-requisite for qualification):		Rev. A	
Die Size (stepping):	64 mils x 67 mils	What ID markings on Die:	7C82640A (CY2254ASC-1) Metal Mask Option 1: 7C82643A (CY2260SC-1) 7C82644A (CY2254ASC-2) 7C82645A (CY2260SC-2) 7C82646A (CY2260SC-3) 7C82647A (CY2252SC-1) 7C82648A (CY2260SC-3H)

TECHNOLOGY/FAB PROCESS DESCRIPTION - LG27			
Number of Metal Layers:	2	Metal Composition:	Metal 1: 500A Ti/1,200A TiW/6,000A Al/1,200A TiW Metal 2: 1,500A TiW//10,000A Al/150A Ti
Passivation Type and Materials:	7000A TEOS + 6000A Si_2N_4		
Free Phosphorus contents in top glass layer(%):	N/A		
Die Coating(s), if used:	N/A		
Generic Process Technology/Design Rule (µ-drawn):	CMOS, Double Poly, Double Metal /0.65 µm		
Gate Oxide Material/Thickness (MOS):	SiO_2 / 145 A		
Name/Location of Die Fab (prime) Facility:	Cypress Semiconductor - Bloomington, MN		
Die Fab Line ID/Wafer Process ID:	Fab3/LG27		

PLASTIC PACKAGE/ASSEMBLY DESCRIPTION			
Package Outline, Type, or Name:	28 Pins, 300 mil SOIC		
Mold Compound Name/Manufacturer:	Sumitomo EME-6300H(R)		
Lead Frame material:	Copper		
Lead Finish, composition:	Solder Plated, 85%Sn, 15%Pb		
Die Attach Area Plating:	Silver Spot		
Die Attach Method:	Paste	Die Attach Material:	Silver Epoxy
Wire Bond Method:	Thermosonic	Wire Material/Size:	Gold / 1.3 mil
JESD22-A12 Moisture Sensitivity Level	Level 1		
Name/Location of Assembly (prime) facility:	Anam, Philippines (PHIL-M)		

CYPRESS
SEMICONDUCTOR
Clock Synthesizer/Driver, LG27 Technology, QTP 95521 V. 2.0

RELIABILITY TESTS PERFORMED

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc = 4.05V, 150°C	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc = 4.05V, 150°C	P
Read and Record Life Test	Dynamic Operating Condition, Vcc = 4.05V, 150°C	P
High Temperature Steady State Life	Static Operating condition, Vcc = 4.05, 150°C	P
High Accelerated Saturation Test	140°C, 85%RH, 3.8V bias Pre-condition: 48 Hrs PCT (121°C, 100% RH)	P
Temperature Cycle, Plastic package	MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C Pre-condition: 48 Hrs PCT (121°C, 100% RH)	P
Electrostatic Discharge Human Body Model (ESD-HMB)	MIL-STD-883C, Method 3015.7	P 2,200V
Electrostatic Discharge Charge Device Model (ESD-CDM)	Cypress Spec. 25-00020	P 1,000V
Latchup Sensitivity	In accordance with JEDEC 17. Positive injection at 8.0V, Negative injection at -5.0V, DC Pre Vcc and Post Vcc test, Power Supply Overvoltage at 8V, test temperature = 125°C	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal[3] A.F	Voltage[4] A.F	Failure Rate
High Temperature Operating Life Early Failure Rate	290 Devices	0	n/a	n/a	n/a	0 PPM
High Temperature Operating Life[1,2] Long Term Failure Rate	58,000 DHRs	0	0.6	82	4.8	43 FITs

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate.
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A = The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

[4] Voltage Acceleration Factor:

$$AF = \text{Exp}[\beta(V_1 - V_2)]$$

Where:

ß = 2
V_1 is the junction voltage of the device under stress and V_2 is the voltage of the device at use conditions.

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RELIABILITY TEST DATA

QTP#: 95521

DEVICE	ASSY-LOC	FABLOT#	ASSYLOT#	DURATION	S/S	REJ	FAIL MODE
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (150C, 4.05V)							
CY2254ASC	PHIL-M	3534417	13151 (SWR)	48	80	0	
CY2254ASC	PHIL-M	3534417	13151 (SWR)	48	210	0	
STRESS: HI-ACCEL SATURATION TEST (140C, 85%RH, 3.8V), PRECONDITION 48 HRS PCT							
CY2254ASC	PHIL-M	3534417	13151 (SWR)	128	45	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST (150C, 4.05V)							
CY2254ASC	PHIL-M	3534417	13151 (SWR)	168	75	0	1 EOS
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (150C, 4.05V)							
CY2254ASC	PHIL-M	3534417	13151 (SWR)	425	116	0	
CY2254ASC	PHIL-M	3534417	13151 (SWR)	500	116	0	
STRESS: READ & RECORD LIFE TEST (150C, 4.05V)							
CY2254ASC	PHIL-M	3534417	13151 (SWR)	48	10	0	
CY2254ASC	PHIL-M	3534417	13151 (SWR)	500	10	0	
STRESS: TEMP CYCLE, COND. C, -65 TO 150C, PRECONDITION 48 HRS PCT							
CY2254ASC	PHIL-M	3534417	13151 (SWR)	300	45	0	
CY2254ASC	PHIL-M	3534417	13151 (SWR)	1000	45	0	