

Cypress Semiconductor Product Qualification Report

QTP# 93332/97316/99211 VERSION 1.0
March, 2000

MAX® EPLD, P20 Technology, Fab 2	
CY7C346	128-Macrocell MAX EPLD

MAX is a Registered Trademark of ALTERA Corporation

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

Ed Russell
Reliability Manager
(408)432-7069

PRODUCT DESCRIPTION (for qualification)			
Qualification Purpose: Qualifies CY7C346 in P20 Technology, Fab2.			
Marketing Part #:	CY7C346		
Package:	84pin Plastic Llead Chip Carriers (PLCC) 84pin Ceramic Windowed J-Leaded Chip Carriers (WLCC) 100pin Ceramic Windowed Pin Grid Arrays (WPGA)		
Device Description:	128-Macrocell MAX EPLD		
Cypress Division:	Cypress Semiconductor Corporation – MPD Division		
Overall Die (or Mask) REV Level (pre-requisite for qualification):	Rev. A		
Die Size (stepping):	335 mils x 289 mils	What ID markings on Die:	Z1031

TECHNOLOGY/FAB PROCESS DESCRIPTION - P20			
Number of Metal Layers:	2	Metal Composition:	Metal 1: 500 Ti/ 1200TiW6K Al/500Ti Metal 2: 1minRF/1500Ti/9KAl
Passivation Type and Materials:	Oxide		
Free Phosphorus contents in top glass layer(%):	0%		
Generic Process Technology/Design Rule (μ -drawn):	CMOS, Double Metal /0.8 μ m		
Gate Oxide Material/Thickness (MOS):	SiO ₂ / 195 Å		
Name/Location of Die Fab (prime) Facility:	Cypress Semiconductor - Round Rock, TX (Fab2)		
Die Fab Line ID/Wafer Process ID:	Fab2/P20		

PLASTIC PACKAGE/ASSEMBLY DESCRIPTION			
Package Outline, Type, or Name:	84pin Plastic Leaded Chip Carrier (PLCC)		
Mold Compound Name/Manufacturer:	NITTO MP-8000CHV		
Lead Frame material:	Copper		
Lead Finish, composition:	Solder Plated, 85%Sn, 15%Pb		
Die Attach Method:	Ag Epoxy	Die Attach Material:	8361 Ablestick
Wire Bond Method:	Au Ball	Wire Material/Size:	Au / 1.3 mil
Thermal Resistance Theta JA	27		
JESD22-A112 Moisture Sensitivity Level:	Level 5		
Name/Location of Assembly (prime) facility:	Cypress Thailand (ALPHA-X)		

HERMETIC PACKAGE/ASSEMBLY DESCRIPTION			
Package Outline, Type, or Name:	84pin Ceramic Windowed J-Leaded Chip Carrier (W LCC) 100pin Ceramic Windowed Pin Grid Arrays (WPGA)		
Lead Frame material:	Kovar		
Lead Finish, composition:	Nickle/Gold Plate		
Die Attach Method:	Ag/Glass	Die Attach Material:	QMI 2419
Wire Bond Method:	Wedge/Ultrasonic	Wire Material/Size:	Al / 1.25 mil
JESD22-A112 Moisture Sensitivity Level:	N/A		
Name/Location of Assembly (prime) facility:	Cypress Bangkok, Thailand (Alpha-X)		

RELIABILITY TESTS PERFORMED

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition Vcc= 125°C/140°C, 5.75V	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc = 140°C/ 5.75V	P
High Accelerated Saturation Test (HAST)	140°C, 5. 5V	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C	P
Data Bake Hermetic Data Bake Plastic	Cypress Spec. 25-00060 (250°C, No Bias) (165°C, No Bias)	P
Input/Output Capacitance	Cypress Spec. 01-00123	P
Internal Water Vapor	MIL-STD-883, Method 1018	P
Latch-up	Cypress Spec. 01-00081	P +/- 200mA

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF⁴	Failure Rate
High Temperature Operating Life Early Failure Rate ¹	984	0	N/A	N/A	0 PPM
High Temperature Operating Life ^{2, 3} Long Term Failure Rate	78,000 DHRs	0	0.7	110	107 FIT

¹ production burn-in of 12 Hrs at 150°C, 5.75V is required for Military products.

²Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.

³Chi-squared 60% estimations used to calculate the failure rate.

⁴Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp \left[\frac{E_A}{k} \left[\frac{1}{T_2} - \frac{1}{T_1} \right] \right]$$

where:

E_A = The Activation Energy of the defect mechanism.

k = Boltzmann's constant = 8.62x10⁻⁵ eV/Kelvin.

T₁ is the junction temperature of the device under stress and T₂ is the junction temperature of the device at use conditions.

RELIABILITY TEST DATA

QTP#: 93332/97316/99211¹

EVAL #	DEVICE	ASSY-LOC	FABLOT#	ASSYLOT#	DURATION	S/S	REJ	FAIL MODE
STRESS: DATA BAKE-HERMETIC (250C, NO BIAS)								
93332	CY7C346-HC	USA-G	2330524	49304892	96	77	0	
93332	CY7C346-HC	USA-G	2330524	49304892	168	77	0	
STRESS: DATA BAKE-PLASTIC (165C, NO BIAS)								
93332	CY7C346-JC	KOREA-A	2333798	49305964	168	76	0	
93332	CY7C346-JC	KOREA-A	2333798	49305964	552	75	0	1 ESD
STRESS: HIGH ACCELERATED SATURATION TEST (140C/5.5V)								
93332	CY7C346-JC	KOREA-A	2333798	49305964	128	46	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (140C, 5.75V)								
93332	CY7C346-HC	USA-G	2330524	49304748	120	78	0	
93332	CY7C346-HC	USA-G	2330524	49304748	1000	78	0	
STRESS: TC COND. C, -65 TO 150C, HERMETIC DEVICES								
93332	CY7C346-JC	KOREA-A	2333798	49305964	300	46	1	1 TOPSIDE CRACKS
93332	CY7C346-HC	USA-G	2330524	49304748	100	47	0	
93332	CY7C346-HC	USA-G	2330524	49304748	1000	47	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (140C, 5.75V)								
97316	CY7C346-HMB	ALPHA-X	2720543	219708428	72	132	0	
97316	CY7C346-RMB	ALPHA-X	2719344	219708446P	72	178	0	
97316	CY7C346-RMB	ALPHA-X	2718201	219708195P	72	185	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (125C, 5.75V)								
99211	CY7C346-JC	ALPHA-X	2910832	619920149	96	193	0	
99211	CY7C346-JC	ALPHA-X	2910382	619915399	96	296	0	1 EOS

¹Combined Reliability Data
 QTP #93332 (Product Qualification)
 QTP #97316 (Military Burn-In reduction)
 QTP #99211 (Commercial Burn-In elimination)