Cypress Semiconductor
Technology Qualification Report

QTP# 91423 VERSION 2.0
July, 2003

16K Chop Redesign	
MARKETING PART NUMBER	**DEVICE DESCRIPTION**
CY7C128A	2K x 8 Static R/W RAM
CY7C167A	16K x 1 Static R/W RAM
CY7C168A	4K x 4 Static RAM
CY7C169A	4K x 4 Static RAM
CY7C170A	4K x 4 Static RAM
CY7C171A	4K x 4 Static R/W, Separate I/O
CY7C172A	4K x 4 Static R/W, Separate I/O

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

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PRODUCT DESCRIPTION (for qualification)

Information provided in this document is intended for generic qualification and technically describes the Cypress part supplied:

Marketing Part #:	CY7C128A		
Device Description:	64K SRAM		
Cypress Division:	Cypress Semiconductor Corporation		
Overall Die (or Mask) REV Level (pre-requisite for qualification):	Rev. F		
What ID markings on Die:	7C128D		
Cypress Qualification completion/Marketing Availability Dates (Current REV):	April/1992	Now	

TECHNOLOGY/FAB PROCESS DESCRIPTION

Number of Metal Layers:	1	Metal Composition:	TiW, 1% SiAl, Ti
Passivation Type and Materials:	7K Teos, 8K Oxynitride		
Free Phosphorus contents in top glass layer(%):	None		
Die Coating(s), if used:	Polyimide		
Generic Process Technology/Design Rule (μ-drawn):	CMOS /0.8 μm		
Gate Oxide Material/Thickness (MOS):	SiO_2 / 145 A		
Name/Location of Die Fab (prime) Facility:	Cypress Semiconductor, Bloomington, MN Cypress Semiconductor, Round Rock, TX		
Die Fab Line ID/Wafer Process ID:	Fab3/R21 Fab2/R21		

PLASTIC PACKAGE/ASSEMBLY DESCRIPTION

Package Outline, Type, or Name:	24-pin,300-mil		
Die to Package edge clearance:	54 mils per side		
Mold Compound Name/Manufacturer:	Sumitomo EME-6300H(R)		
Lead Frame material:	Copper		
Lead Finish, composition:	Solder Dipped, 63%Sn, 37%Pb		
Die Attach Area Plating:	Silver	Die Attach Pad Dim:	160 mils x 160 mils
Die Attach Method:	Epoxy	Die Attach Material:	Silver Epoxy
Wire Bond Method:	Thermocompression	Wire Material/Size:	Gold / 1.3 mil
Name/Location of Assembly (prime) facility:	Cypress Semiconductor, Bangkok, Thailand		
Assembly Line ID and Process ID:	ALPHA-X / P24310		

HERMETIC PACKAGE/ASSEMBLY DESCRIPTION			
Package Outline, Type, or Name:	24-pin, 300-mil CerDIP		
Die to Package edge clearance:	51 mils per side		
Mold Compound Name/Manufacturer:	N/A		
Lead Frame material:	Alloy 42		
Lead Finish, composition:	Solder Dipped, 63%Sn, 37%Pb		
Die Attach Area Plating:	None	Die Attach Pad Dim:	170 mils x 270 mils
Die Attach Method:	Paste	Die Attach Material:	Silver Glass
Wire Bond Method:	Ultrasonic	Wire Material/Size:	Aluminum / 1.25 mil
Name/Location of Assembly (prime) facility:	Cypress Semiconductor, Bangkok, Thailand		
Assembly Line ID and Process ID:	ALPHA-X/D243B		

OTHER INFORMATION

For approval by similarity, identify other devices using the same basic die with bonding or metal mask options or test selections and explain:

CY7C167A/CY7C168A/CY7C169A/CY7C170A/CY7C171A/CY7C172A

If Cypress is planning any changes in the near future, identify change (Qtr/Yr) in:			
Die Design Rev./Shrink:		Die Process Change:	
Fab/Assembly site change:		Cross Licensee/Licensor:	
Other Devices to be qualified in this technology:			
Other Packages to be qualified for this device:		LCC/SOJ	
ESD Voltage Rating (per MIL STD-008, Method 3018):		>2,000V	
Flammability Classification (UL-94V):	1/8 or None		
Alternate Fab/Assembly Locations:	Fab: Fab3 - Bloomington, MN Fab2 - Round Rock, TX Assembly: Omedata, Indonesia		

Please attach the following Qualification / Reliability data for the die revision and Package type, for the fab and assembly sites identified above (mark [X] if included):

1	x	HAST (5.5V, 130°C, 85%RH, 15psig)	7	x	Operating Life at (temp):	150°C
2		Temperature Cycles (-65°C to 150°C)	8	x	Steady State Life (HTSSL, 5.75V, 150°C)	
3	x	Temperature Cycles (-40°C to 165°C)	9		Temperature Humidity Bias (5.5V, 85°C, 85%RH)	
4		Data Retention Bake, Plastic (165°C)	10	x	Latchup Testing	
5		Data Retention Bake, Hermetic (250°C)	11	x	ESD Tests (MIL-STD 883, method 3015)	
6	x	Autoclave (PCT, 121°C, 100%RH)	12		Other:	

PRODUCT INFORMATION FOR QUALIFICATION BY SIMILARITY

Product Family: 16K SRAM

Mfg Division: Cypress Semiconductor

Supplier's Part Number	Rate Speed (ns)	Pkg Size/ Type	Die Rev.	Die Size mil x mil (stepping)	Design Rule (µ)	Fabrication		Passivation Type	Mold Compound	Assembly Line Location	ESD Volt Rating
						Process ID	Line ID				
CY7C128A -**PC -**VC -**DMB -**LMB	15 ns to 45 ns	24.3 PDIP 24L SOJ 24.3 CDIP 24R LCC	F	143 x 120	0.8mµ	CMOS	2,3	LTO + Oxynitride	Sumitomo	Cypress-Bangkok, Thailand	>2,000V HMB
CY7C167A -**PC -**VC -**DMB	15 ns to 45 ns	20.3 PDIP 20L SOJ 20.3 CDIP	F	143 x 120	0.8mµ	CMOS	2,3	LTO + Oxynitride	Sumitomo	Cypress-Bangkok, Thailand	>2,000V HMB
CY7C168A -**PC -**VC -**DMB	15 ns to 45 ns	20.3 PDIP 20L SOJ 20.3 CDIP	F	143 x 120	0.8mµ	CMOS	2,3	LTO + Oxynitride	Sumitomo	Cypress-Bangkok, Thailand	>2,000V HMB
CY7C169A -**PC -**VC	15 ns to 35ns	20.3 PDIP 20L SOJ	F	143 x 120	0.8mµ	CMOS	2,3	LTO + Oxynitride	Sumitomo	Cypress-Bangkok, Thailand	>2,000V HMB
CY7C170A -**PC -**VC -**DMB	15 ns to 35 ns	22.3 PDIP 24L SOJ 22.3 CDIP	F	143 x 120	0.8mµ	CMOS	2,3	LTO + Oxynitride	Sumitomo	Cypress-Bangkok, Thailand	>2,000V HMB
CY7C171A -**PC -**VC -**DMB -**LMB	15 ns to 45 ns	24.3 PDIP 24L SOJ 24.3 CDIP 24S LCC	F	143 x 120	0.8mµ	CMOS	2,3	LTO + Oxynitride	Sumitomo	Cypress-Bangkok, Thailand	>2,000V HMB
CY7C172A -**PC -**VC -**DMB -**LMB	15 ns to 45 ns	24.3 PDIP 24L SOJ 24.3 CDIP 24S LCC	F	143 x 120	0.8mµ	CMOS	2,3	LTO + Oxynitride	Sumitomo	Cypress-Bangkok, Thailand	>2,000V HMB

DEVICE RELIABILITY SUMMARY

Marketing Part: CY7C128A
Pkg Description: PDIP, CDIP
Wafer Fab: Fab 3 - Bloomington, Mn
Assembly: Cypress - San Jose, CA

High Temperature Dynamic Operating Life (HTOL, 5.75V, 150°C) - Early Failure Rate						
Device	Assy Lot#	Fab Lot #	48 Hours			Cumulative
7C128F	73190	3139553	0/406			0/2111
7C128F	74591	3141589	0/1605			

High Temperature Dynamic Operating Life (HTOL, 5.75V, 150°C) - Latent Failure Rate						
Device	Assy Lot#	Fab Lot #	80 Hours	500 Hours		Cumulative
7C128F	73190	3139553	0/346	0/346		0/702
7C128F	74591	3141589	0/356	0/356		

High Temperature Steady State Life Test (HTSSL, 5.75V, 150°C)						
Device	Assy Lot#	Fab Lot #	80 Hours	168 Hours		Cumulative
7C128F	73190	3139553	0/128	128		0/257
7C128F	74591	3141589	0/129	129		

Temperature Cycle (Condition C, -40°C to 125C)						
Device	Assy Lot#	Fab Lot #	300 Cycles	1000 Cycles		Cumulative
7C128F	73190	3139553	0/77	0/77		0/144
7C128F	74591	3141589	0/67	0/67		

Autoclave (PCT, No bias, 121°C, 100%RH, 15psig)						
Device	Assy Lot#	Fab Lot #	168 Hours			Cumulative
7C128F	73190	3139553	0/45			0/45

DEVICE RELIABILITY SUMMARY

Marketing Part:	CY7C128A	Wafer Fab:	Fab 3 - Bloomington, Mn
Pkg Description:	PDIP, CDIP	Assembly:	Cypress - San Jose, CA

High Accelerated Saturation Test (HAST, 5.5V, 130°C, 85%RH, 15psig)						
Device	Assy Lot#	Fab Lot #	100 Hours			Cumulative
7C128F	73190	3139553	0/45			0/45

Group C, Subgroup 1, Life Test (HTOL, 5.75V, 150°C)						
Device	Assy Lot#	Fab Lot#	184 Hours			Cumulative
7C128F-DMB	78463	3203915	0/79			0/79

DEVCIE RELIABILITY SUMMARY

16K Chop Re-design		
CY7C128A/167A/168A/169A/170A/171A/172A		
Electrostatic Discharge		
Human Body Model Circuit per Mil Std 883, Method 3015		
>+2000V	Unit 1	>-2000V
>+2000V	Unit 2	>-2000V
>+2000V	Unit 3	>-2000V
(Highest passing voltage, +10% Guard-banded)		

Latchup
Testing to Cypress Internal Latch-up Procedure
Current Injection = 200mA Trigger
Hot Socket = V_{CC} 0 - 8V
Temp = 125°C

DEVICE RELIABILITY SUMMARY

Marketing Part:	CY7C128A	Wafer Fab:	Fab2, Round Rock, TX
Pkg Description:	24-pin, 300-mil PDIP 24-pin, 300-mil CDIP	Assembly:	Cypress-Bangkok, Thailand

High Temperature Dynamic Operating Life (HTOL, 7.0V, 125°C) - Early Failure Rate						
Device	Assy Lot#	Fab Lot #	12 Hours			Cumulative
7C128F-PC	219301438	2316617	0/3440			0/6623
7C128F-PC	219301439	2316417	0/3183			

Group C, Subgroup 1, Life Test (HTOL, 5.75V, 150°C)						
Device	Assy Lot#	Fab Lot#	184 Hours			Cumulative
7C128F-DMB	219301783	2316417	0/132			0/132