Cypress Semiconductor
Product Qualification Report

QTP# 060908 VERSION 3.1
February 2009

36 Meg QDR/DDR Synchronous SRAM Family R9Q-3R Technology, Fab4	
CY7C1243V18 CY7C1245V18	36-Mbit QDR™-II+ SRAM 4-Word Burst Architecture (2.0 Cycle Read Latency)
CY7C1248V18 CY7C1250V18	36-Mbit DDR™-II+ SRAM 2-Word Burst Architecture (2.0 Cycle Read Latency)
CY7C1263V18 CY7C1265V18	36-Mbit QDR™-II+ SRAM 4-Word Burst Architecture (2.5 Cycle Read Latency)
CY7C1268V18 CY7C1270V18	36-Mbit DDR™-II+ SRAM 2-Word Burst Architecture (2.5 Cycle Read Latency)
CY7C1413JV18 CY7C1415JV18 CY7C1426JV18	36-Mbit QDR™-II SRAM 4-Word Burst Architecture (1.5 Cycle Read Latency)
CY7C1418JV18 CY7C1420JV18	36-Mbit DDR™-II SRAM 2-Word Burst Architecture (1.5 Cycle Read Latency)
CY7C1414JV18	36-Mbit QDR™-II SRAM 2-Word Burst Architecture (1.5 Cycle Read Latency)
CY7C1425JV18	36-Mbit QDR™-II SRAM 2-Word Burst Architecture (1.5 Cycle Read Latency)
CY7C1423JV18	36-Mbit DDR-II SIO SRAM 2-Word Burst Architecture

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

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PRODUCT QUALIFICATION HISTORY

Qual Report	Description of Qualification Purpose	Date Comp
033302	New Technology R9T-3R, Fab 4 and New Device CY7C137*/138*E, 18 Meg Synchronous product family	Sep 04
044201	R9 36 Meg QDR, 7C1414B 4 Metal Layer Process	May 05
063206	R9 36 Meg QDR MM1 New Mask Qualification	Sep 06
063903	R9 36 Meg QDR/DDR B-4 Baja Fix Mask Qualification	Jan 07
060908	Qualify R9 36 Meg QDRII (Smaller or Same Die Area/Density), Fab4	Jan 07
081001	Qualify 7C1423J/U Bond Option Using 7C1273A/B (QDR2+) Silicon	May 08
083809	R9 7C1273AC 36M QDRII+ Fast A1 Output Register Noise and Decoupling Design Fix Mask Qualification	Oct 08
082702	Qualify R9 36 Meg QDRII Bond Option CY7C1414J/CY7C1415J	Feb 09

PRODUCT DESCRIPTION (for qualification)	
Purpose: Qualify 36Meg QDR/DDR (Smaller die) Synchronous product family in qualified technology R9Q-3R, Fab 4	
Marketing Part #:	CY7C1243/5V18, CY7C1248/50V18, CY7C1263/5V18, CY7C1268/70V18, CY7C1413/26JV18, CY7C1418/20/25JV18, CY7C1423JV18
Device Description:	1.8V / 2.5V, Commercial and Industrial available in 165-Ball FBGA
Cypress Division:	Cypress Semiconductor Corporation –Memory & Image Division (MID)

TECHNOLOGY/FAB PROCESS DESCRIPTION R9Q-3R			
Number of Metal Layers:	4	Metal Composition:	Metal 1: 150Å Ti / 3200Å Al / 300Å TiW Metal 2: 150Å Ti / 6000Å Al / 300Å TiW Metal 3: 150Å Ti / 6000Å Al / 300Å TiW Metal 4: 150Å Ti / 8000Å Al / 300Å TiW
Passivation Type and Materials:		1000Å Oxide TEOS / 9000Å Nitride	
Generic Process Technology/Design Rule (-drawn):		CMOS, Quad Metal, 90 nm	
Gate Oxide Material/Thickness (MOS):		Nitridized SiO_2, Thin GOX 20A, Thick GOX, 58A	
Name/Location of Die Fab (prime) Facility:		Cypress Semiconductor – Bloomington, MN	
Die Fab Line ID/Wafer Process ID:		Fab4/R9Q-3R	

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY SITE FACILITY
165-Ball FBGA	**TAIWAN-G**

Note: Package Qualification details upon request

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	BB165
Package Outline, Type, or Name:	165-Ball Thin Ball Grid Array (FBGA)
Mold Compound Name/Manufacturer:	KE-G2270 / Kyocera
Mold Compound Flammability Rating:	VO UL-94
Mold Compound Alpha Emission Rate:	<0.001C/cm^2-hr
Oxygen Rating Index:	N/A
Lead Frame Material:	Substrate, BT
Lead Finish, Composition / Thickness:	Sn63%, Pb37%
Die Backside Preparation Method/Metallization:	Grinding
Die Separation Method:	Sawing
Die Attach Supplier:	Ablestik
Die Attach Material:	2025D
Die Attach Method:	Epoxy
Bond Diagram Designation:	001-44423
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au, 1.0 mil
Thermal Resistance Theta JA °C/W:	16.1°C/W
Package Cross Section Yes/No:	No
Assembly Process Flow:	001-06520
Name/Location of Assembly (prime) facility:	ASE-Taiwan
MSL Level	3
Reflow Profile	220C

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	ChipMOS-Taiwan (GO)

Note: Please contact a Cypress Representative for other packages availability

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc Max (Core) = 2.25V, 150°C Dynamic Operating Condition, Vcc Max (Core) = 2.25V, 125°C	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc Max (Core)= 2.25V, 150°C	P
High Temperature Steady State Life	Static Operating Condition, Vcc Max = 2.25V, 150°C	P
Low Temperature Operating Life	Dynamic Operating Condition, Vcc = 6.50V, -30°C	P
High Accelerated Saturation Test (HAST)	130°C, 3.63V, 85%RH Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C/60%RH+3IR-Reflow, **220°C**+0, -5°C	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C/60%RH+3IR-Reflow, **220°C**+0, -5°C	P
Pressure Cooker	121°C, 100%RH, 15 Psig Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C/60%RH+3IR-Reflow, **220°C**+0, -5°C	P
High Temperature Storage	150°C, no bias	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V MIL-STD-883, Method 3015.7	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V JEDEC EIA/JESD22-A114-E	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V Cypress Spec. 25-00020	P
Current Density	Cypress Spec 22-00029	P
Age Bond Strength	200°C, 4HRS MIL-STD-883, Method 883-2011	P
Acoustic Microscopy	Cypress Spec. 25-00104	P
Bond Pull	Cypress Spec. 12-00292	P
Ball Shear	Cypress Spec. 24-00018	P
Dynamic Latch up	Cypress Spec. 01-00081	P
Internal Visual	Cypress Spec. 12-00292	P
Static Latch up	125C, ± 200/240mA Cypress Spec. 01-00081	P
Thermal Shock	125C, -55C Cypress Spec. 25-00014	P
X-Ray	Cypress Spec. 12-00292	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[3]	Failure Rate
High Temperature Operating Life Early Failure Rate	1,535 Devices	0	N/A	N/A	0 PPM
High Temperature Operating Life[1,2] Long Term Failure Rate	485,000 DHRs	0	0.7	170	11 FIT

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate..
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

Where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

Reliability Test Data

QTP #: 033302

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC-MSL3							
CY7C1470V33 (7C1470A)	4330156	*610417279*	CML-R	COMP	15	0	
CY7C1470V33 (7C1470A)	4321389	*610417280*	CML-R	COMP	15	0	
CY7C1470V33 (7C1470A)	4323794	*610348235*	TAIWN-G	COMP	15	0	
STRESS: AGE BOND STRENGTH							
CY7C1370DV33 (7C1370E)	4421235	*610447674*	CML-R	COMP	5	0	
CY7C1370DV33 (7C1370E)	4406200	*610435906*	CML-R	COMP	5	0	
CY7C1370DV33 (7C1370E)	4410258	*610437891*	CML-R	COMP	5	0	
STRESS: BALL SHEAR							
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	COMP	10	0	
STRESS: BOND PULL							
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	COMP	10	0	
STRESS: DYNAMIC LATCH-UP							
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V							
CY7C1470V33 (7C1470A)	4352888	*610425832*	TAIWN-G	COMP	3	0	
CY7C1470V33 (7C1470A)	4401980	*610425833*	TAIWN-G	COMP	3	0	
CY7C1370DV33 (7C1370E)	4345377	*610417723*	CML-R	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114-B, 2,200V							
CY7C1470V33 (7C1470A)	4352888	*610425832*	TAIWN-G	COMP	9	0	
CY7C1470V33 (7C1470A)	4401980	*610425833*	TAIWN-G	COMP	9	0	
CY7C1370DV33 (7C1370E)	4421235	*610446833*	CML-R	COMP	9	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C1470V33 (7C1470A)	4352888	*610425832*	TAIWN-G	COMP	9	0	
CY7C1470V33 (7C1470A)	4401980	*610425833*	TAIWN-G	COMP	9	0	
CY7C1370DV33 (7C1370E)	4345377	*610417723*	CML-R	COMP	9	0	
STRESS: HIGH TEMPERATURE STORAGE, PLASTIC, 150C							
CY7C1470V33 (7C1470A)	4323794	*610348234*	TAIWN-G	500	47	0	
CY7C1470V33 (7C1470A)	4323794	*610348234*	TAIWN-G	1000	47	0	

Reliability Test Data

QTP #: 033302

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 150C, 2.25V, Vcc Max (Core)							
CY7C1370DV33 (7C1370E)	4345377	*610424939*	CML-R	48	193	0	
CY7C1370DV33 (7C1370E)	4345377	*610422227*	CML-R	48	951	0	
CY7C1370DV33 (7C1370E)	4406200	*610435906*	CML-R	48	1246	0	
CY7C1370DV33 (7C1370E)	4410258	*610437891*	CML-R	48	1382	1	NON-VISUAL
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 150C, 2.25V, Vcc Max (Core)							
CY7C1370DV33 (7C1370E)	4345377	*610424939*	CML-R	500	170	0	
CY7C1370DV33 (7C1370E)	4406200	*610435906*	CML-R	500	400	0	
CY7C1370DV33 (7C1370E)	4410258	*610437891*	CML-R	500	400	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST, 150C, 2.25V, Vcc Max							
CY7C1470V33 (7C1470A)	4405088	*610418824*	TAIWN-G	80	85	0	
CY7C1470V33 (7C1470A)	4405088	*610418824*	TAIWN-G	168	85	0	
STRESS: INTERNAL VISUAL							
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	COMP	5	0	
STRESS: LOW TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, -30C, 6.50V, Vcc							
CY7C1470V33 (7C1470A)	4333765	*610349455*	CML-R	500	45	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1370DV33 (7C1370E)	4345377	*610422227*	CML-R	168	50	0	
CY7C1370DV33 (7C1370E)	4406200	*610435906*	CML-R	168	50	0	
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	168	43	0	
STRESS: HI-ACCEL SATURATION TEST, 130C, 85%RH, 3.63V, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1370DV33 (7C1370E)	4406200	*610435906*	CML-R	128	50	0	
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	128	47	0	
CY7C1470V33 (7C1470A)	4330156	*610417279*	CML-R	128	44	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 7.5V, +/-300mA							
CY7C1470V33 (7C1470A)	4352888	*610425832*	TAIWN-G	COMP	3	0	
CY7C1470V33 (7C1470A)	4401980	*610425833*	TAIWN-G	COMP	3	0	
CY7C1370DV33 (7C1370E)	4345377	*610417723*	CML-R	COMP	3	0	

Reliability Test Data

QTP #: 033302

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: TC COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY7C1370DV33 (7C1370E)	4345377	*610422227*	CML-R	300	50	0	
CY7C1370DV33 (7C1370E)	4345377	*610422227*	CML-R	500	49	0	
CY7C1370DV33 (7C1370E)	4345377	*610422227*	CML-R	1000	49	0	
CY7C1470V33 (7C1470A)	4330156	*610417279*	CML-R	300	43	0	
CY7C1470V33 (7C1470A)	4330156	*610417279*	CML-R	500	43	0	
CY7C1470V33 (7C1470A)	4330156	*610417279*	CML-R	1000	42	0	
CY7C1470V33 (7C1470A)	4321389	*610417280*	CML-R	300	34	0	
CY7C1470V33 (7C1470A)	4321389	*610417280*	CML-R	500	33	0	
CY7C1470V33 (7C1470A)	4321389	*610417280*	CML-R	1000	33	0	
STRESS: THERMAL SHOCK							
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	100	46	0	
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	200	46	0	
STRESS: X-RAY							
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	COMP	15	0	

Reliability Test Data

QTP #: 044201

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C1415AV18 (7C1415B)	4448196	*610507735*	TAIWN-G	COMP	15	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114-B, 2,200V							
CY7C1414AV18 (7C1414B)	4447043	*610505881*	TAIWN-G	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V							
CY7C1414AV18 (7C1414B)	4447043	*610505881*	TAIWN-G	COMP	3	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, 2.25V, Vcc Max (Core)							
CY7C1413AV18 (7C1413B)	4453505	*610516129*	TAIWN-G	96	265	0	
CY7C1413AV18 (7C1413B)	4452210	*610513131*	TAIWN-G	96	970	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1414AV18 (7C1414B)	4447043	*610505881*	TAIWN-G	168	48	0	
CY7C1414AV18 (7C1414B)	4447043	*610505881*	TAIWN-G	288	48	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 6.0V, +/-300mA							
CY7C1414AV18 (7C1414B)	4447043	*610505881*	TAIWN-G	COMP	3	0	
STRESS: TC COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY7C1414AV18 (7C1414B)	4447043	*610505881*	TAIWN-G	300	48	0	
CY7C1414AV18 (7C1414B)	4447043	*610505881*	TAIWN-G	500	48	0	
CY7C1414AV18 (7C1414B)	4447043	*610505881*	TAIWN-G	1000	48	0	

Reliability Test Data

QTP #: 060908

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C1265V18 (7C1265AC)	4613010	*610642236*	TAIWN-G	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114-B, 2,200V							
CY7C1265V18 (7C1265AC)	4613010	*610642236*	TAIWN-G	COMP	9	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 3.0V, +/-200mA							
CY7C1265V18 (7C1265AC)	4613010	*610642236*	TAIWN-G	COMP	3	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, 2.25V, Vcc Max (Core)							
CY7C1265V18 (7C1265AC)	4634954	*610664363*	TAIWN-G	96	1535	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1265V18 (7C1265AC)	4551740	*610613815N1*	TAIWN-G	168	47	0	
CY7C1265V18 (7C1265AC)	4551740	*610613815N1*	TAIWN-G	288	47	0	
STRESS: TC COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY7C1265V18 (7C1265AC)	4551740	*610613815N1*	TAIWN-G	300	46	0	
CY7C1265V18 (7C1265AC)	4551740	*610613815N1*	TAIWN-G	500	45	0	
CY7C1265V18 (7C1265AC)	4551740	*610613815N1*	TAIWN-G	1000	44	0	

Reliability Test Data

QTP #: 081001

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C1423JV18 (7C1423JC)	4737994	610809664	TAIWN-G	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114-E, 2,200V							
CY7C1423JV18 (7C1423JC)	4737994	610809664	TAIWN-G	COMP	8	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 2.85V, +/-200mA							
CY7C1423JV18 (7C1423JC)	4737994	610809664	TAIWN-G	COMP	6	0	

Reliability Test Data

QTP #: 083809

Device	Fab Lot #	Assy Lot #	Assy Loc	Wafer #	Samp	Rej	Failure Mechanism
STRESS: E-TEST YIELD							
CY7C1270V18 (7C1270XC)	4833244	N/A	N/A	1-9		COMPARABLE	
STRESS: SORT YIELD							
CY7C1270V18 (7C1270XC)	4833244	610844176	N/A	1-9		COMPARABLE	