Cypress Semiconductor
Product Qualification Report

QTP# 060802 VERSION 1.0
April 2006

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<tr><td>CY505YC64DT</td><td>Clock Generator for Intel® Broadwater Chipset</td></tr>
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CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

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TECHNOLOGY QUALIFICATION HISTORY

Qual Report	Description of Qualification Purpose	Date Comp
024604	R52T-3 Technology Process Derivative Qual	May 03
040903	New Device B30M (CY28437) Base Die in R52T-3 Technology	Feb 05
060802	CY505YC64DT Rev. D Mask/Bond Option from qualified B30M Base Die in R52T-3 Technology	Apr 06

PRODUCT DESCRIPTION (for qualification)	
Qualification Purpose: CY505YC64DT Rev. D Mask/Bond Option from qualified B30M Base Die in R52T-3 Technology	
Marketing Part #:	CY505YC64DT
Device Description:	3.3V, Clock Generator for Intel® Broadwater Chipset available in 64-Pin TSSOP
Cypress Division:	Cypress Semiconductor Corporation –Consumer & Computation Division (CCD)
Overall Die (or Mask) REV Level (pre-requisite for qualification):	Rev. D
What ID markings on Die:	CY7C8B012A

TECHNOLOGY/FAB PROCESS DESCRIPTION - R52T-3			
Number of Metal Layers:	3	Metal Composition:	Metal 1: 500Å TiW / 6000Å Al / 500Å TiW Metal 2: 500Å TiW / 6000Å Al / 500Å TiW Metal 3: 300Å Ti / 8000Å Al / 300Å TiW
Passivation Type and Materials:	1000Å SiO2 / 9000Å Si3N4		
Free Phosphorus contents in top glass layer (%):	0%		
Number of Transistors in Device	44,000		
Number of Gates in Device	5,500		
Generic Process Technology/Design Rule (μ-drawn):	CMOS – Triple Metal, 0.25μm		
Gate Oxide Material/Thickness (MOS):	SiO_2, 55Å		
Name/Location of Die Fab (prime) Facility:	Cypress Semiconductor -- Bloomington, MN		
Die Fab Line ID/Wafer Process ID:	Fab4/R52T-3		

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY SITE FACILITY
64-Lead TSSOP	**PHIL-M**

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	ZZ64
Package Outline, Type, or Name:	64-Pin Thin Shrunk Small Outline Packages
Mold Compound Name/Manufacturer:	Sumitomo G700K
Mold Compound Flammability Rating:	V-O per UL94
Oxygen Rating Index:	NA
Lead Frame Material:	Copper
Lead Finish, Composition / Thickness:	NiPdAu
Die Backside Preparation Method/Metallization:	Wafer Backgrind
Die Separation Method:	100% Saw
Die Attach Supplier:	Ablestik
Die Attach Material:	Ablebond 8290
Die Attach Method:	Epoxy Cure
Bond Diagram Designation	001-03062
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au. 1.0mil
Thermal Resistance Theta JA °C/W:	61.19°C/W
Package Cross Section Yes/No:	N/A
Assembly Process Flow:	49-24999
Name/Location of Assembly (prime) facility:	Amkor-Phil (PHIL-M)
Moisture Level/Profile	**MSL3/260C**

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	**CML-R**
Fault Coverage:	100%

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc Max = 3.8V, 125°C	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc Max = 3.8V, 125°C	P
High Accelerated Saturation Test (HAST)	130°C, 3.63V, 85%RH Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30C/60%RH+3IR-Reflow, 220°C+0, -5°C	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30C/60%RH+3IR-Reflow, 220°C+0, -5°C Precondition: JESD22 Moisture Sensitivity MSL 1 168 Hrs, 85C/85%RH+3IR-Reflow, 260°C+0, -5°C	P
Pressure Cooker	121°C, 100%RH Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30C/60%RH+3IR-Reflow, 220°C+0, -5°C Precondition: JESD22 Moisture Sensitivity MSL 1 168 Hrs, 85C/85%RH+3IR-Reflow, 260°C+0, -5°C	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V JESD22, Method A114-B	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V MIL-STD-883, Method 3015.7	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V Cypress Spec. 25-00020	P
Acoustic Microscopy	Cypress Spec. 25-00104	P
Static Latch-up	125C, ± 200mA/± 300mA Cypress Spec. 01-00081	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[4]	Failure Rate
High Temperature Operating Life Early Failure Rate	4,377 Devices	0	N/A	N/A	0 PPM
High Temperature Operating Life[1,2] Long Term Failure Rate	547,000 DHRs	0	0 .7	55	30 FITs

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate.
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

Reliability Test Data

QTP #: 024604

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC-, MSL3							
CY6981-BA (7C6981A)	4223346	*610243127/3004*	TAIWN-G	COMP	18	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (125C, 3.8V, Vcc Max)							
CY6981-BA (7C6981A)	4147861	*610221501/2/27521*	TAIWN-G	96	1342	0	
CY6981-BA (7C6981A)	4238026	*610250542*	TAIWN-G	96	1020	0	
CY6981-BA (7C6981A)	4223346	*610243127/3004/7*	TAIWN-G	96	1015	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (125C, 3.8V, Vcc Max)							
CY6981-BA (7C6981A)	4147861	*610221501/2*	TAIWN-G	168	182	0	
CY6981-BA (7C6981A)	4147861	*610221501/2*	TAIWN-G	500	182	0	
CY6981-BA (7C6981A)	4147861	*610221501/2*	TAIWN-G	1000	182	0	
CY6981-BA (7C6981A)	4223346	*610243127/3004*	TAIWN-G	168	182	0	
CY6981-BA (7C6981A)	4223346	*610243127/3004*	TAIWN-G	500	182	0	
CY6981-BA (7C6981A)	4223346	*610243127/3004*	TAIWN-G	1000	180	0	
CY6981-BA (7C6981A)	4238026	*610250542*	TAIWN-G	168	368	0	
CY6981-BA (7C6981A)	4238026	*610250542*	TAIWN-G	500	368	0	
STRESS: ESD-CHARGE DEVICE MODEL (500V)							
CY6981-BA (7C6981A)	4147861	*610221501/2/2752*	TAIWN-G	COMP	9	0	
CY6981-BA (7C6981A)	4223346	*610243127/3004*	TAIWN-G	COMP	9	0	
ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015 (2,200V)							
CY6981-BA (7C6981A)	4147861	*610221501/2/2752*	TAIWN-G	COMP	9	0	
CY6981-BA (7C6981A)	4223346	*610243127/3004*	TAIWN-G	COMP	9	0	
STRESS: STATIC LATCH-UP TESTING (125C, 10V, +/-300mA)							
CY6981-BA (7C6981A)	4147861	*610221501/2/2752*	TAIWN-G	COMP	3	0	
CY6981-BA (7C6981A)	4238026	*610250542*	TAIWN-G	COMP	3	0	
STRESS: PRESSURE COOKER TEST, (121C, 100%RH), PRE COND 192 HR 30C/60%RH, MSL3							
CY6981-BA (7C6981A)	4147861	*610221501/2/2752*	TAIWN-G	168	50	0	
CY6981-BA (7C6981A)	4223346	*610243127/3004*	TAIWN-G	168	48	0	
CY6981-BA (7C6981A)	4223346	*610243127/3004*	TAIWN-G	288	48	0	
CY6981-BA (7C6981A)	4238026	*610250542*	TAIWN-G	168	48	0	
CY6981-BA (7C6981A)	4238026	*610250542*	TAIWN-G	288	48	0	

Reliability Test Data

QTP #: 024604

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HI-ACCEL SATURATION TEST (130C, 85%RH, 3.63V), PRE COND 192 HR 30C/60%RH, MSL3							
CY6981-BA (7C6981A)	4147861	*610221501/2/2752*	TAIWN-G	128	50	0	
CY6981-BA (7C6981A)	4223346	*610243127/3004*	TAIWN-G	128	47	0	
STRESS: TC COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY6981-BA (7C6981A)	4147861	*610221501/2/2752*	TAIWN-G	300	50	0	
CY6981-BA (7C6981A)	4147861	*610221501/2/2752*	TAIWN-G	500	50	0	
CY6981-BA (7C6981A)	4147861	*610221501/2/2752*	TAIWN-G	1000	50	0	
CY6981-BA (7C6981A)	4223346	*610243127/3004*	TAIWN-G	300	48	0	
CY6981-BA (7C6981A)	4223346	*610243127/3004*	TAIWN-G	500	48	0	
CY6981-BA (7C6981A)	4223346	*610243127/3004*	TAIWN-G	1000	48	0	
CY6981-BA (7C6981A)	4238026	*610250542*	TAIWN-G	300	48	0	
CY6981-BA (7C6981A)	4238026	*610250542*	TAIWN-G	500	48	0	
CY6981-BA (7C6981A)	4238026	*610250542*	TAIWN-G	1000	48	0	

Reliability Test Data

QTP #: 040903

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY28437OXCT (7C828437A)	4444247	*610463705*	CML-R	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JESD22, METHOD A114-B, 2,200V							
CY28437OXCT (7C828437A)	4444247	*610463705*	CML-R	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V							
CY28437OXCT (7C828437A)	4444247	*610463705*	CML-R	COMP	3	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, 3.8V, Vcc Max							
CY28437OXCT (7C828437A)	4444247	*610463705*	CML-R	96	442	0	
CY28437OXCT (7C828437A)	4444247	*610463737*	CML-R	96	260	0	
CY28437OXCT (7C828437A)	4444247	*610463736*	CML-R	96	298	0	
STRESS: PRESSURE COOKER TEST, (121C, 100%RH), PRE COND 168 HR 85C/85%RH, MSL1							
CY28437OXCT (7C828437A)	4444247	*610463705*	CML-R	168	45	0	
STRESS: STATIC LATCH-UP TESTING (125C, 8.48V, +/-300mA)							
CY28437OXCT (7C828437A)	4444247	*610463705*	CML-R	COMP	3	0	
STRESS: TC COND. C -65C TO 150C, PRE COND 168 HR 85C/85%RH, MSL1							
CY28437OXCT (7C828437A)	4444247	*610463705*	CML-R	300	45	0	

Reliability Test Data

QTP #: 060802

Device	*Fab Lot #*	*Assy Lot #*	*Assy Loc*	*Duration*	*Samp*	*Rej*	*Failure Mechanism*
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY505YC64DT (7C885052D)	4602891	*610610207*	PHIL-M	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JESD22, METHOD A114-B, 2,200V							
CY505YC64DT (7C885052D)	4602891	*610610207*	PHIL-M	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V							
CY505YC64DT (7C885052D)	4602891	*610610207*	PHIL-M	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING (125C, 5.42V, +/-200mA)							
CY505YC64DT (7C885052D)	4602891	*610610207*	PHIL-M	COMP	3	0	