Cypress Semiconductor
Technology Qualification Report

QTP# 054605 VERSION 1.0
March 2006

P26 TLM Technology Transfer to Magnachip	
CY7C63722 **CY7C63723** **CY7C63743**	**enCoRe™ USB Combination Low-Speed USB and PS/2 Peripheral Controller**

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

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QUALIFICATION HISTORY

Qual Report	Description of Qualification Purpose	Date Comp
054605	P26 TLM Technology at Magnachip	Mar 06

PRODUCT DESCRIPTION (for qualification)		
Qualification Purpose: Qualify P26 TLM Technologyat Magnachip		
Marketing Part #:	CY7C63722, CY7C63723, CY7C62743	
Device Description:	enCoRe™ USB Combination Low-Speed USB abd PS/2 Peripheral Controller	
Cypress Division:	Cypress Semiconductor Corporation –Consumer and Computation Division (CCD)	
Overall Die (or Mask) REV Level (pre-requisite for qualification):		Rev. A
What ID markings on Die:	7C6370A	

TECHNOLOGY/FAB PROCESS DESCRIPTION - P26			
Number of Metal Layers:	3	Metal Composition:	Metal 1: 1500Å TiW / 4000Å Al / 750Å TiW Metal 2: 1500Å TiW / 4000Å Al / 750Å TiW Metal 3: 1500Å TiW / 8000Å Al / 750Å TiW
Passivation Type and Materials:		Oxynitride	
Generic Process Technology/Design Rule (µ-drawn):		CMOS, Double Metal/0.65µm	
Gate Oxide Material/Thickness (MOS):		SiO_2, 165Å	
Name/Location of Die Fab (prime) Facility:		Magnachip/Cheong-Ju-Korea	
Die Fab Line ID/Wafer Process ID:		Fab2/P26	

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY SITE FACILITY
18/24-Lead PDIP	**INDNS-O**
24-Lead QFN	**CML-R**
24-Lead SOP	**CML-R**

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	PZ24
Package Outline, Type, or Name:	24-Pin (300mil) Lead-Free PDIP
Mold Compound Name/Manufacturer:	MP8000CH
Mold Compound Flammability Rating:	V-0
Oxygen Rating Index:	N/A
Lead Frame Material:	Cu
Lead Finish, Composition / Thickness:	100% Matte Sn
Die Backside Preparation Method/Metallization:	Backgrind
Die Separation Method:	Saw
Die Attach Supplier:	Ablestik
Die Attach Material:	8361
Die Attach Method:	Epoxy
Bond Diagram Designation:	001-05902
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au. 1.0 mil
Thermal Resistance Theta JA °C/W:	86.9°C/W
Package Cross Section Yes/No:	N/A
Assembly Process Flow:	001-03750
Name/Location of Assembly (prime) facility:	INDNS-O

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	**CML-R, INDNS-O**
Fault Coverage:	100%

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc Max = 5.75V, 150°C	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc Max = 5.75V, 150°C	P
Long Life Verification	Dynamic Operating Condition, Vcc Max = 5.75V, 150°C	P
High Accelerated Saturation Test (HAST)	130°C, 5.75V, 85%RH	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C	P
Pressure Cooker	121°C, 100%RH	P
Aged Bond Strength	MIL-STD-883, Method 2011	P
Data Retention (Plastic)	165C, non-biased	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V JESD22, Method A114-B	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V MIL-STD-883, Method 3015.7	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V Cypress Spec. 25-00020	P
Static Latch-up	125C, ± 200mA In accordance with JEDEC 17. Cypress Spec. 01-00081	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[4]	Failure Rate
High Temperature Operating Life Early Failure Rate	1,021Devices	0	N/A	N/A	0 PPM
High Temperature Operating Life[1,2] Long Term Failure Rate	187,184 DHRs	0	0 .7	170	29 FITs

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate.
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

Reliability Test Data

QTP #: 054605

Device	Fab Lot #	Assy Lot#	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: AGE BOND STRENGTH							
CY7C63743C (7C637402A)	2552760	*510600403*	INDNS-O	COMP	10	0	
CY7C63743C (7C637402A)	2602103	*510600521*	INDNS-O	COMP	10	0	
CY7C63743C (7C637402A)	2602104	*510600522*	INDNS-O	COMP	10	0	
STRESS: DATA RETENTION, 165C, no bias							
CY7C63743C (7C637402A)	2552760	*510600403*	INDNS-O	168	80	0	
CY7C63743C (7C637402A)	2552760	*510600403*	INDNS-O	552	80	0	
CY7C63743C (7C637402A)	2602103	*510600521*	INDNS-O	168	82	0	
CY7C63743C (7C637402A)	2602103	*510600521*	INDNS-O	552	82	0	
STRESS: ESD-CHARGE DEVICE MODEL, (500V)							
CY7C63743C (7C637402A)	2552760	*510600403*	INDNS-O	COMP	9	0	
CY7C63743C (7C637402A)	2602103	*510600521*	INDNS-O	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JESD22, METHOD A114-B, (2,200V)							
CY7C63743C (7C637402A)	2552760	*510600403*	INDNS-O	COMP	9	0	
CY7C63743C (7C637402A)	2602103	*510600521*	INDNS-O	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V							
CY7C63743C (7C637402A)	2552760	*510600403*	INDNS-O	COMP	3	0	
CY7C63743C (7C637402A)	2602103	*510600521*	INDNS-O	COMP	3	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (150C, 5.75V), Vcc Max)							
CY7C63743C (7C637402A)	2552760	*510600403*	INDNS-O	64	335	0	
CY7C63743C (7C637402A)	2602103	*510600521*	INDNS-O	48	335	0	
CY7C63743C (7C637402A)	2602104	*510600522*	INDNS-O	48	351	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (150C, 5.75V), Vcc Max)							
CY7C63743C (7C637402A)	2552760	*510600403*	INDNS-O	100	240	0	
CY7C63743C (7C637402A)	2552760	*510600403*	INDNS-O	269	240	0	
CY7C63743C (7C637402A)	2602103	*510600521*	INDNS-O	256	239	0	
CY7C63743C (7C637402A)	2602104	*510600522*	INDNS-O	256	240	0	
STRESS: HI-ACCEL SATURATION TEST (130C, 85%RH, 5.75V)							
CY7C63743C (7C637402A)	2552760	*510600403*	INDNS-O	128	48	0	
CY7C63743C (7C637402A)	2602103	*510600521*	INDNS-O	128	51	0	

Reliability Test Data

QTP #: 054605

Device	Fab Lot #	Assy Lot#	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: PRESSURE COOKER TEST (121C, 100%RH)							
CY7C63743C (7C637402A)	2552760	*510600403*	INDNS-O	168	50	0	
CY7C63743C (7C637402A)	2602103	*510600521*	INDNS-O	168	50	0	
STRESS: STATIC LATCH-UP TESTING (125C, 8.5V, +/-200mA)							
CY7C63743C (7C637402A)	2552760	*510600403*	INDNS-O	COMP	3	0	
CY7C63743C (7C637402A)	2602103	*510600521*	INDNS-O	COMP	3	0	
STRESS: TC COND. C -65C TO 150C							
CY7C63743C (7C637402A)	2552760	*510600403*	INDNS-O	300	50	0	
CY7C63743C (7C637402A)	2602103	*510600521*	INDNS-O	300	50	0	
CY7C63743C (7C637402A)	2602104	*510600522*	INDNS-O	300	50	0	