Cypress Semiconductor
Product Qualification Report

QTP# 051901 VERSION 3.2
May 2008

72 Meg QDR Synchronous SRAM Family R9Q-3R Technology, Fab4	
CY7C1510V18 CY7C1512V18 CY7C1514V18 CY7C1525V18	72-Mbit QDR™ - II SRAM 2-Word Burst Architecture
CY7C1511V18 CY7C1513V18 CY7C1515V18 CY7C1526V18	72-Mbit QDR™ - II SRAM 4-Word Burst Architecture
CY7C1516V18 CY7C1518V18 CY7C1520V18 CY7C1527V18	72-Mbit DDR-II SRAM 2-Word Burst Architecture
CY7C1517V18 CY7C1519V18 CY7C1521V18 CY7C1528V18	72-Mbit DDR-II SRAM 4-Word Burst Architecture
CY7C1522V18 CY7C1523V18 CY7C1524V18 CY7C1529V18	72-Mbit DDR-II SIO SRAM 2-Word Burst Architecture

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

Zhaomin Ji
Principal Reliability Engineer
(408) 432-7021

Mira Ben-Tzur
Quality Engineering Director
(408) 943-2675

PRODUCT QUALIFICATION HISTORY

Qual Report		Description of Qualification Purpose	Date Comp
033302		New Technology R9T-3R, Fab 4, and New Device CY7C137*/138*E (18Meg) Synchronous product family	Sept 04
051207		R9 18 Meg QDR, 7C1313D 4 Metal Layer Process	Mar 05
051901		New Device CY7C151*/7C152* AC (72Meg QDR/DDR/LW) Device Family, R9Q-3R Technology fabricated at Fab4	May 05

Cypress products are manufactured using qualified processes. The technology qualification for this product is referenced above and must be considered to get a complete and thorough evaluation of the reliability of the product.

PRODUCT DESCRIPTION (for qualification)	
Qualification Purpose:	Qualify CY7C1513A, 72Meg QDR Synchronous product family in R9Q-3R Technology, Fab 4
Marketing Part #:	CY7C1510/2/4/25V18, CY7C1511/3/5/26V18, CY7C1516/8/20/27V18, CY7C1517/9/21/28V18, CY7C1522/3/4/9V18
Device Description:	1.8V / 2.5V, Commercial and Industrial available in 165-Ball FBGA
Cypress Division:	Cypress Semiconductor Corporation –Memory & Image Division (MID)
Overall Die (or Mask) REV Level (pre-requisite for qualification):	Rev. A
What ID markings on Die:	7C1513A

TECHNOLOGY/FAB PROCESS DESCRIPTION – R9Q-3R			
Number of Metal Layers:	4	Metal Composition:	Metal 1: 150Å Ti /3200Å Al / 300Å TiW Metal 2: 150Å Ti /6000 Å Al / 300Å TiW Metal 3: 150Å Ti / 6000Å Al / 300Å TiW Metal 4: 150Å Ti / 8000Å Al / 300Å TiW
Passivation Type and Materials:	1000Å Oxide TEOS / 9000Å Nitride		
Free Phosphorus contents in top glass layer(%):	N/A		
Number of Transistors in Device	~ 504M		
Number of Logic Gates in Device	~ 72M		
Generic Process Technology/Design Rule (μ-drawn):	CMOS, Quad Metal, 90 nm		
Gate Oxide Material/Thickness (MOS):	Nitridized SiO_2, Thin GOX 20A, Thick GOX, 58A		
Name/Location of Die Fab (prime) Facility:	Cypress Semiconductor -- Bloomington, MN		
Die Fab Line ID/Wafer Process ID:	Fab4/R9Q-3R		

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY SITE FACILITY
165-Ball FBGA	**ASE-Taiwan (G)**

Note: Package Qualification details upon request

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	BB165
Package Outline, Type, or Name:	165-Ball Thin Ball Grid Array (FBGA)
Mold Compound Name/Manufacturer:	KE-G2270 / Kyocera
Mold Compound Flammability Rating:	V-0 per UL94
Oxygen Rating Index:	N/A
Lead Frame Material:	Substrate, BT
Lead Finish, Composition / Thickness:	Sn 63%, Pb 37%
Die Backside Preparation Method/Metallization:	Grinding
Die Separation Method:	Sawing
Die Attach Supplier:	Ablestik
Die Attach Material:	2025D
Die Attach Method:	Epoxy
Bond Diagram Designation:	10-05399
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au, 1.0 mil
Thermal Resistance Theta JA °C/W:	18.8°C/W
Package Cross Section Yes/No:	No
Assembly Process Flow:	49-41041
Name/Location of Assembly (prime) facility:	ASE-Taiwan

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	ChipMOS-Taiwan (GO)
Fault Coverage:	100%

Note: Please contact a Cypress Representative for other packages availability

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc Max (Core) = 2.25V, 125°C Dynamic Operating Condition, Vcc Max (Core) = 2.25V, 150°C	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc Max (Core) = 2.25V, 125°C Dynamic Operating Condition, Vcc Max (Core) = 2.25V, 150°C	P
High Temperature Steady State Life	Static Operating Condition, Vcc Max= 2.25V, 150°C	P
Low Temperature Operating Life	Dynamic Operating Condition, Vcc = 6.50V, -30°C	P
High Accelerated Saturation Test (HAST)	130°C, 3.63V,85%RH Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C/60%RH+3IR-Reflow, **260°C**+0, -5°C	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C/60%RH+3IR-Reflow, **260°C**+0, -5°C	P
Pressure Cooker	121°C, 100%RH, 15 Psig Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C/60%RH+3IR-Reflow**, 260°C**+0, -5°C	P
High Temperature Storage	150°C ± 5°C, no bias	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V MIL-STD-883, Method 3015.7	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V JEDEC EIA/JESD22-A114-B	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V Cypress Spec. 25-00020	P
Current Density	Cypress Spec 22-00029	P
Age Bond Strength	200°C, 4HRS MIL-STD-883, Method 883-2011	P
Acoustic Microscopy	Cypress Spec. 25-00104	P
Dynamic Latchup	In accordance with JEDEC 17. Cypress Spec. 01-00081	P
Static Latchup	125C, ± 300mA In accordance with JEDEC 17. Cypress Spec. 01-00081	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[3]	Failure Rate
High Temperature Operating Life Early Failure Rate	1,613 Devices	0	N/A	N/A	0 PPM
High Temperature Operating Life[1,2] Long Term Failure Rate	696,000 DHRs	0	0.7	55	24 FIT

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate..
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

Reliability Test Data

QTP #: 033302

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC, MSL3							
CY7C1470V33 (7C1470A)	4330156	*610417279*	CML-R	COMP	15	0	
CY7C1470V33 (7C1470A)	4321389	*610417280*	CML-R	COMP	15	0	
CY7C1470V33 (7C1470A)	4323794	*610348235*	TAIWN-G	COMP	15	0	
STRESS: AGE BOND STRENGTH							
CY7C1370DV33 (7C1370E)	4421235	*610447674*	CML-R	COMP	5	0	
CY7C1370DV33 (7C1370E)	4406200	*610435906*	CML-R	COMP	5	0	
CY7C1370DV33 (7C1370E)	4410258	*610437891*	CML-R	COMP	5	0	
STRESS: BALL SHEAR							
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	COMP	10	0	
STRESS: BOND PULL							
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	COMP	10	0	
STRESS: DYNAMIC LATCH-UP							
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V							
CY7C1470V33 (7C1470A)	4352888	*610425832*	TAIWN-G	COMP	3	0	
CY7C1470V33 (7C1470A)	4401980	*610425833*	TAIWN-G	COMP	3	0	
CY7C1370DV33 (7C1370E)	4345377	*610417723*	CML-R	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114-B, 2,200V							
CY7C1470V33 (7C1470A)	4352888	*610425832*	TAIWN-G	COMP	9	0	
CY7C1470V33 (7C1470A)	4401980	*610425833*	TAIWN-G	COMP	9	0	
CY7C1370DV33 (7C1370E)	4421235	*610446833*	CML-R	COMP	9	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C1470V33 (7C1470A)	4352888	*610425832*	TAIWN-G	COMP	9	0	
CY7C1470V33 (7C1470A)	4401980	*610425833*	TAIWN-G	COMP	9	0	
CY7C1370DV33 (7C1370E)	4345377	*610417723*	CML-R	COMP	9	0	
STRESS: HIGH TEMPERATURE STORAGE, PLASTIC, 150C							
CY7C1470V33 (7C1470A)	4323794	*610348234*	TAIWN-G	500	47	0	
CY7C1470V33 (7C1470A)	4323794	*610348234*	TAIWN-G	1000	47	0	

Reliability Test Data

QTP #: 033302

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 150C, 2.25V, Vcc Max (Core)							
CY7C1370DV33 (7C1370E)	4345377	*610424939*	CML-R	48	193	0	
CY7C1370DV33 (7C1370E)	4345377	*610422227*	CML-R	48	951	0	
CY7C1370DV33 (7C1370E)	4406200	*610435906*	CML-R	48	1246	0	
CY7C1370DV33 (7C1370E)	4410258	*610437891*	CML-R	48	1382	1	Non-Visual
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 150C, 2.25V, Vcc Max (Core)							
CY7C1370DV33 (7C1370E)	4345377	*610424939*	CML-R	500	170	0	
CY7C1370DV33 (7C1370E)	4406200	*610435906*	CML-R	500	400	0	
CY7C1370DV33 (7C1370E)	4410258	*610437891*	CML-R	500	400	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST, 150C, 2.25V, Vcc Max							
CY7C1470V33 (7C1470A)	4405088	*610418824*	TAIWN-G	80	85	0	
CY7C1470V33 (7C1470A)	4405088	*610418824*	TAIWN-G	168	85	0	
STRESS: INTERNAL VISUAL							
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	COMP	5	0	
STRESS: LOW TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, -30C, 6.50V, Vcc							
CY7C1470V33 (7C1470A)	4333765	*610349455*	CML-R	500	45	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1370DV33 (7C1370E)	4345377	*610422227*	CML-R	168	50	0	
CY7C1370DV33 (7C1370E)	4406200	*610435906*	CML-R	168	50	0	
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	168	43	0	
STRESS: HI-ACCEL SATURATION TEST, 130C, 85%RH, 3.63V, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1370DV33 (7C1370E)	4406200	*610435906*	CML-R	128	50	0	
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	128	47	0	
CY7C1470V33 (7C1470A)	4330156	*610417279*	CML-R	128	44	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 7.5V, +/300mA							
CY7C1470V33 (7C1470A)	4352888	*610425832*	TAIWN-G	COMP	3	0	
CY7C1470V33 (7C1470A)	4401980	*610425833*	TAIWN-G	COMP	3	0	
CY7C1370DV33 (7C1370E)	4345377	*610417723*	CML-R	COMP	3	0	

Reliability Test Data

QTP #: 033302

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: TC COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY7C1370DV33 (7C1370E)	4345377	*610422227*	CML-R	300	50	0	
CY7C1370DV33 (7C1370E)	4345377	*610422227*	CML-R	500	49	0	
CY7C1370DV33 (7C1370E)	4345377	*610422227*	CML-R	1000	49	0	
CY7C1470V33 (7C1470A)	4330156	*610417279*	CML-R	300	43	0	
CY7C1470V33 (7C1470A)	4330156	*610417279*	CML-R	500	43	0	
CY7C1470V33 (7C1470A)	4330156	*610417279*	CML-R	1000	42	0	
CY7C1470V33 (7C1470A)	4321389	*610417280*	CML-R	300	34	0	
CY7C1470V33 (7C1470A)	4321389	*610417280*	CML-R	500	33	0	
CY7C1470V33 (7C1470A)	4321389	*610417280*	CML-R	1000	33	0	
STRESS: THERMAL SHOCK							
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	100	46	0	
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	200	46	0	
STRESS: X-RAY							
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	COMP	15	0	

Reliability Test Data

QTP #: 051207

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C1314BV18 (7C1314D)	4444085	*610507866*	TAIWN-G	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114-B, 2,200V							
CY7C1314BV18 (7C1314D)	4444085	*610507866*	TAIWN-G	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V							
CY7C1314BV18 (7C1314D)	4444085	*610507866*	TAIWN-G	COMP	3	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, 2.25V, Vcc Max (Core)							
CY7C1312BV18 (7C1312D)	4440030	*610465503*	TAIWN-G	96	1803	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 125C, 2.25V, Vcc Max (Core)							
CY7C1312BV18 (7C1312D)	4440030	*610465503*	TAIWN-G	168	1395	0	
CY7C1312BV18 (7C1312D)	4440030	*610465503*	TAIWN-G	500	359	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1313BV18 (7C1313D)	4436152	*610459993*	TAIWN-G	168	50	0	
CY7C1313BV18 (7C1313D)	4436152	*610459993*	TAIWN-G	288	50	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 4.5V, +/300mA							
CY7C1314BV18 (7C1314D)	4444085	*610507866*	TAIWN-G	COMP	3	0	
STRESS: TC COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY7C1313BV18 (7C1313D)	4436152	*610459993*	TAIWN-G	300	50	0	
CY7C1313BV18 (7C1313D)	4436152	*610459993*	TAIWN-G	500	50	0	
CY7C1313BV18 (7C1313D)	4436152	*610459993*	TAIWN-G	1000	50	0	

Reliability Test Data

QTP #: 051901

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C1514V18 (7C1514A)	4412759	*610452856*	TAIWN-G	COMP	9	0	
CY7C1515V18 (7C1515A)	4347629	*610436891*	TAIWN-G	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V							
CY7C1512V18 (7C15121A)	4406161	*610437889*	TAIWN-G	COMP	3	0	
CY7C1515V18 (7C1515A)	4347629	*610436891*	TAIWN-G	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114-B, 2,200V							
CY7C1512V18 (7C15121A)	4406161	*610437889*	TAIWN-G	COMP	9	0	
CY7C1515V18 (7C1515A)	4347629	*610436891*	TAIWN-G	COMP	6	0	
CY7C1514V18 (7C1514A)	4412759	*610452856*	TAIWN-G	COMP	6	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, 2.25V, Vcc Max (Core)							
CY7C1512V18 (7C15121A)	4451052	*610510951*	TAIWN-G	96	1613	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 125C, 2.25V, Vcc Max (Core)							
CY7C1512V18 (7C15121A)	4425371	*61059092*	TAIWN-G	168	862	0	
CY7C1512V18 (7C15121A)	4425371	*61059092*	TAIWN-G	500	612	0	
CY7C1512V18 (7C15121A)	4422351	*61059094*	TAIWN-G	168	696	0	
CY7C1512V18 (7C15121A)	4422351	*61059094*	TAIWN-G	500	696	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1512V18 (7C15121A)	4413923	*610445193*	TAIWN-G	168	48	0	
CY7C1512V18 (7C15121A)	4413923	*610445193*	TAIWN-G	288	48	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 5.0V, +/300mA							
CY7C1512V18 (7C15121A)	4406161	*610437889*	TAIWN-G	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 5.5V, +/300mA							
CY7C1515V18 (7C1515A)	4347629	*610436891*	TAIWN-G	COMP	6	0	
STRESS: TC COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY7C1512V18 (7C15121A)	4413923	*610445193*	TAIWN-G	300	48	0	
CY7C1512V18 (7C15121A)	4413923	*610445193*	TAIWN-G	500	48	0	
CY7C1512V18 (7C15121A)	4413923	*610445193*	TAIWN-G	1000	48	0	