Cypress Semiconductor
Qualification Report

QTP# 051501 VERSION 1.0
May 2005

Cypress Minnesota (CMI) Sort Site Qualification	
2 Meg, 3V PSRAM Device **PowerChip 0.165µm**	
K002MC5BW	**2Mb (128K X 16) Pseudo Static RAM Die**
GC2016V5BW	**2Mb (128K X 16) Pseudo Static RAM Die**

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

Rene Rodgers
Principal Reliability Engineer
(408) 943-2732

Sabbas Daniel
Quality Engineering Director
408) 943-2685

PRODUCT QUALIFICATION HISTORY

Qual Report		Description of Qualification Purpose		Date Comp
050707		Qualify Cypress Minnesota (CMI) as an additional Sort Site for K008MC2AW (8 Meg) Device Family		Mar 05
051501		Qualify Cypress Minnesota (CMI) as an additional Sort Site for K002MC5BW (2 Meg) Device Family (by extension)		May 05

PRODUCT DESCRIPTION (for qualification)	
Qualification Purpose: Qualify Cypress Minnesota (CMI) as an additional Sort Site for K002MC5BW device family	
Marketing Part #:	CYK128K16SCCB/CYK128K16MCCB/WCMC2016V9B/WCMC2016V7B
Device Description:	128K X 16, 3V, Industrial Temp product available in die and 48 Ball BGA
Cypress Division:	Cypress Semiconductor Corporation – Memory Product Division

TECHNOLOGY/FAB PROCESS DESCRIPTION			
Number of Metal Layers:	2	Metal Composition:	Metal 1: TiN/Ti (18/8.5nm) Metal 2: TiN/Alcu/TiN (23/800/28nm)
Passivation Type and Materials:			Si3N4 & Polyimide
Free Phosphorus contents in top glass layer (%):			0%
Number of Transistors in Device:			36 Million
Number of Gates in Device			1.5 Million
Generic Process Technology/Design Rule (µ-drawn):			0.16um + Stack Capacitor
Gate Oxide Material/Thickness (MOS):			SiO_2 / 72A
Name/Location of Die Fab (prime) Facility:			Powerchip Semiconductor Corp, HsinChu, Taiwan
Die Fab Line ID/Wafer Process ID:			BF04301

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
Final Sort Yield	Fisher’s Exact Test w/ $\alpha < 0.05$	P
Bin to Bin Correlation	Exact Bin from both Test Locations	P

Reliability Test Data

QTP #: 050707

Device	Fab Lot #	Wafer#	Chipmos Yield	CMI Yield	Rej	Failure Mechanism
STRESS: SORT 1 TEST YIELD						
K008MC1AW	9447414	WAFER 1	2190	2193		
		WAFER 3	2146	2110		
		WAFER 5	2197	2148		
K008MC1AW	9447407	WAFER 1	1814	1832		
		WAFER 3	2123	2118		
		WAFER 5	2137	2128		
K008MC1AW	9446363	WAFER 1	2143	2086		
		WAFER 3	2171	2163		
		WAFER 5	2206	2190		
STRESS: SORT 2 TEST YIELD						
K008MC1AW	9447414	WAFER 7	1494	1467		
		WAFER 9	1152	1130		
		WAFER 11	1469	1455		
K008MC1AW	9447407	WAFER 7	1396	1375		
		WAFER 9	1293	1277		
		WAFER 11	1171	1141		
K008MC1AW	9446363	WAFER 7	1833	1778		
		WAFER 9	1685	1573		
		WAFER 11	1716	1646		

As required by Cypress Spec 25-00106, a Fisher's Exact test (F-Test) was performed on the final yield data from both sites. In comparing the final yield data from both sites the F-Test proved that they have the same variance.

STRESS: Bin-to-Bin CORRELATION

Complete. Sample Pass/Fail die chosen at random belonged to the same bin at both test sites.

Reliability Test Data

QTP #: 051501

Device	Fab Lot #	Wafer#	Chipmos Yield	CMI Yield	Rej	Failure Mechanism
STRESS: SORT 1 TEST YIELD						
K002MC5BW	9446353	WAFER 1	5613	5578		
		WAFER 3	5555	5548		
STRESS: F- TEST ANALYSIS ON SORT 1 YIELD						
K002MC5BW	9446353	WAFER 1 & 3	5584	5563		
STRESS: SORT 2 TEST YIELD						
K002MC5BW	9440579	WAFER 5	5166	5178		
		WAFER 7	5100	5122		
STRESS: F- TEST ANALYSIS ON SORT 2 YIELD						
K002MC5BW	9446353	WAFER 5 & 7	5133	5150		
STRESS: FINAL TEST YIELD						
K002MC5BW	9440579	WAFER 5	4984	5160		
		WAFER 7	4817	4817		
STRESS: F- TEST ANALYSIS ON FINAL TEST YIELD						
K002MC5BW	9446353	WAFER 5 & 7	4901	4989		

As required by Cypress Spec 25-00106, a Fisher's Exact test (F-Test) was performed on the final yield data from both sites. In comparing the final yield data from both sites the F-Test proved that they have the same variance.

STRESS: Bin-to-Bin CORRELATION

Complete. Sample Pass/Fail die chosen at random belonged to the same bin at both test sites.