Cypress Semiconductor
Product Qualification Report

QTP# 032105 VERSION 5.0
May 2004

18 Meg QDR/DDR Sync SRAM R7FFT-18, Fab4	
CY7C1303AV18 CY7C1306AV18	18-Mb Burst of 2 Pipelined SRAM with QDR™ Architecture
CY7C1305AV18 CY7C1307AV18	18-Mb Burst of 4 Pipelined SRAM with QDR™ Architecture
CY7C1302BV25 / CY7C1302CV25	9-Mb Burst of 2 Pipelined SRAM with QDR™ Architecture
CY7C1304BV25 / CY7C1304CV25	9-Mb Burst of 4 Pipelined SRAM with QDR™ Architecture
CY7C1308BV25 / CY7C1308CV25	9-Mb 4-Word Burst SRAM with DDR™-I Architecture
CY7C1322V25 / CY7C1322AV25 CY7C1397V25 / CY7C1397AV25	18-Mb 2-Word Burst SRAM with DDR-I Architecture
CY7C1310V18 / CY7C1310AV18 CY7C1312V18 / CY7C1312AV18 CY7C1314V18 / CY7C1314AV18	18-Mb QDR™ -II SRAM Two-word Burst Architecture
CY7C1311V18 / CY7C1311AV18 CY7C1313V18 / CY7C1313AV18 CY7C1315V18 / CY7C1315AV18	18-Mb QDR™ -II SRAM 4-Word Burst Architecture
CY7C1316V18 / CY7C1316AV18 CY7C1318V18 / CY7C1318AV18 CY7C1320V18 / CY7C1320AV18	18-Mb DDR-II SRAM Two-word Burst Architecture
CY7C1317V18 / CY7C1317AV18 CY7C1319V18 / CY7C1319AV18 CY7C1321V18 / CY7C1321AV18	18-Mb DDR-II SRAM Four-word Burst Architecture
CY7C1392V18 / CY7C1392AV18 CY7C1393V18 / CY7C1393AV18 CY7C1394V18 / CY7C1394AV18	18-Mb DDR-II SIO SRAM Two-word Burst Architecture
CY7C1303V25 / CY7C1303AV25 CY7C1306V25 / CY7C1306AV25	18 Mb Burst of 2 Pipelined SRAM with QDR Architecture
CY7C1305V25 / CY7C1305AV25 CY7C1307V25 / CY7C1307AV25	18 Mb Burst of 4 Pipelined SRAM with QDR Architecture
CY7C1323V25 / CY7C1323AV25 CY7C1398V25 / CY7C1398AV25	18-Mb 4-Word Burst SRAM with DDR-I Architecture

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

Mira Ben-Tzur
Principal Reliability Engineer
(408) 943-2675

PRODUCT QUALIFICATION HISTORY

Qual Report		**Description of Qualification Purpose**		**Date Comp**
032105		Qualify 18 Meg QDR/DDR Synchronous SRAM device qual, CY7C1313V18 family and options on R7FFT-18 Technology		Aug 03
034209		7C1313 165 FBGA (13 x 15 x 1.4mm) 4 Layer Substrate with NSMD & 0.55mm Solder Ball and 7mil Die Thickness		Feb 04
040604		R7 QDR Family Design Change – M1/VIA/M2 Mask Change		Feb 04
041305		Device Name change for R7 QDR Family (M1/VIA/M2) Mask Change		Mar 04

Cypress products are manufactured using qualified processes. The technology qualification for this product is referenced above and must be considered to get a complete and thorough evaluation of the reliability of the product.

PRODUCT DESCRIPTION (for qualification)		
Qualification Purpose: Qualify new CY7C1313V18 family and options in R7FFT-18, Fab 4		
Marketing Part #:	CY7C1310/1/2/3/4/5/6/7/8/9/20/21V18, CY7C1392/3/4V18,CY7C1302/3/4/5/6/7V25, CY7C1322/23V25, CY7C1397/8V25	
Device Description:	3.3V, Commercial available in 165-ball FBGA package.	
Cypress Division:	Cypress Semiconductor Corporation - Memory Product Division (MPD)	
Overall Die (or Mask) REV Level (pre-requisite for qualification):		Rev. C
What ID markings on Die:	7C1305A	

TECHNOLOGY/FAB PROCESS DESCRIPTION – R7FFT-18			
Number of Metal Layers:	3	Metal Composition:	Metal 1: 150Å Ti / 4,230Å Al / 300Å TiW Metal 2: 150Å Ti / 4,230 Å Al / 300Å TiW Metal 3: 150Å Ti / 8,000 Å Al / 300Å TiW
Passivation Type and Materials:		700Å TEOS over M3 / 7000Å Nitride over Oxide	
Free Phosphorus contents in top glass layer(%):		0%	
Number of Transistors in Device		≈115 million	
Number of Gates in Device		≈30 million	
Generic Process Technology/Design Rule (-drawn):		0.15 um	
Gate Oxide Material/Thickness (MOS):		SiO_2, 32Å	
Name/Location of Die Fab (prime) Facility:		Cypress Semiconductor -- Bloomington, MN	
Die Fab Line ID/Wafer Process ID:		Fab4/R7FFT-1.8	

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY SITE FACILITY
165-ball FBGA	**ASE Taiwan (TAIWN-G)**

Note: Package Qualification details upon request

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	BB165
Package Outline, Type, or Name:	165 lead Thin Ball Grid Array (FBGA) 13x15x1.2mm
Mold Compound Name/Manufacturer:	Plaskon SMT-B-IN
Mold Compound Flammability Rating:	V-O per UL94
Oxygen Rating Index:	>34%
Substrate Material	BT Resin
Lead Finish, Composition / Thickness:	Solder Ball, 63%Sn, 37%Pb
Die Backside Preparation Method/Metallization:	Backgrind
Die Separation Method:	Wafer Dicing
Die Attach Supplier:	Ablestik
Die Attach Material:	8355F
Die Attach Method:	Epoxy
Bond Diagram Designation:	10-04782
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au, 1.0um
Thermal Resistance Theta JA °C/W:	16.7°C/W
Package Cross Section Yes/No:	N/A
Assembly Process Flow:	49-41020/49-1020M
Name/Location of Assembly (prime) facility:	ASE-Taiwan (TAIWN-G)

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	Chipmos Taiwan
Fault Coverage:	100%

Note: Please contact a Cypress Representative for other packages availability

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc Max = 2.07V, 125C Dynamic Operating Condition, Vcc Max = 2.07V, 150C	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc Max= 2.07V, 125C Dynamic Operating Condition, Vcc Max =2.07V, 150C	P
High Accelerated Saturation Test (HAST)	130C, 2.07V, 85%RH Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30C/60%RH+3IR-Reflow, 220C+5, 0C	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65C to 150C Precondition: JESD22 Moisture Sensitivity MSL3 192 Hrs, 30C/60%RH+3IR-Reflow, 220C+5, 0C	P
Pressure Cooker	121C, 100%RH Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30C/60%RH+3IR-Reflow, 220C+5, 0C	P
High Temperature Storage	150C ± 5C no bias	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V Cypress Spec. 25-00020	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V MIL-STD-883, Method 3015.7	P
Acoustic Microscopy, MSL 3	Cypress Spec. 25-00104	P
Dynamic Latch-up	125C, 3V	P
Static Latchup	125C, 6.5V, ± 300mA In accordance with JEDEC 17. Cypress Spec. 01-00081	P
Ball Shear	Cypress Spec 12-00292	P
Bond Pull	Cypress Spec 12-00292	P
Die Shear	Cypress Spec 12-00292	P
External Visual	Cypress Spec. 12-00292	P
Physical Dimensions	Cypress Spec. 25-00031	P
Internal Visual	Cypress Spec 25-00017	P
Thermal Shock	MIL-STD-883C, Method 1011, Condition B, -55°C, +125°C	P
X-Ray	Cypress Spec 12-000292	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[3]	Failure Rate
High Temperature Operating Life Early Failure Rate[1]	451 @125C	0	N/A	N/A	0 PPM
High Temperature Operating Life Early Failure Rate[1]	2245 @150C	0	N/A	N/A	0 PPM
High Temperature Operating Life[1,2] Long Term Failure Rate	266,258 DHRs	0	0.7	170	20 FIT

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate..
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

Reliability Test Data

QTP #: 032105

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC - MICROSCOPE, MSL3							
CY7C1313V18	4244530	610300545	TAIWN-G	COMP	15	0	
CY7C1313V18	4247903	610308014	TAIWN-G	COMP	15	0	
CY7C1313V18	4312665	610325607	TAIWN-G	COMP	15	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 150C, 2.07V, Vcc Max							
CY7C1313V18	4244530	610300545	TAIWN-G	72	708	0	
CY7C1313V18	4244530	610253788	TAIWN-G	72	380	0	
CY7C1313V18	4247903	610308014	TAIWN-G	48	784	0	
CY7C1313V18	4303979	610311492	TAIWN-G	48	373	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, 2.07V, Vcc Max							
CY7C1313V18	4312665	610325607	TAIWN-G	48	191	0	
CY7C1313V18	4315181	610326838	TAIWN-G	48	260	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 150C, 2.07V, Vcc Max							
CY7C1313V18	4244530	610300545	TAIWN-G	80	409	0	
CY7C1313V18	4244530	610300545	TAIWN-G	500	409	0	
CY7C1313V18	4303979	610311492	TAIWN-G	80	249	0	
CY7C1313V18	4303979	610311492	TAIWN-G	80	157	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 125C, 2.07V, Vcc Max							
CY7C1313V18	4312665	610325607	TAIWN-G	80	184	0	
CY7C1313V18	4312665	610325607	TAIWN-G	500	184	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C1313V18	4244530	610300545	TAIWN-G	COMP	9	0	
CY7C1313V18	4247903	610308014	TAIWN-G	COMP	9	0	
CY7C1313V18	4312665	610325607	TAIWN-G	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V							
CY7C1313V18	4247903	610308014	TAIWN-G	COMP	9	0	
CY7C1313V18	4312665	610325607	TAIWN-G	COMP	9	0	

Reliability Test Data

QTP #: 032105

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: STATIC LATCH-UP TESTING, 125C, 6.5V, +/300mA							
CY7C1313V18	4244530	610300545	TAIWN-G	COMP	3	0	
CY7C1313V18	4247903	610308014	TAIWN-G	COMP	3	0	
CY7C1313V18	4312665	610325607	TAIWN-G	COMP	3	0	
STRESS: DYNAMIC LATCH-UP TESTING, 3V, +/300mA							
CY7C1313V18	4247903	610308014	TAIWN-G	COMP	4	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1313V18	4247903	610308014	TAIWN-G	168	49	0	
CY7C1313V18	4312665	610325607	TAIWN-G	168	50	0	
STRESS: HI-ACCEL SATURATION TEST, 130C, 85%RH, 3.3V, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1313V18	4244530	610300545	TAIWN-G	128	45	0	
CY7C1313V18	4244530	610300545	TAIWN-G	256	45	0	
CY7C1313V18	4247903	610308014	TAIWN-G	128	48	0	
STRESS: TC COND. C -65C TO 150C, PRECONDITION 192 HRS 30C/60%RH, MSL3							
CY7C1313V18	4244530	610300545	TAIWN-G	300	46	0	
CY7C1313V18	4244530	610300545	TAIWN-G	500	46	0	
CY7C1313V18	4244530	610300545	TAIWN-G	1000	46	0	
CY7C1313V18	4247903	610308014	TAIWN-G	300	49	0	
CY7C1313V18	4247903	610308014	TAIWN-G	500	49	0	
CY7C1313V18	4312665	610325607	TAIWN-G	300	50	0	

Reliability Test Data

QTP #: 034209

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC - MICROSCOPE, MSL3							
CY7C1313V18	4331321	610344833	TAIWN-G	COMP	15	0	
CY7C1313V18	4331321	610344834	TAIWN-G	COMP	15	0	
CY7C1313V18	4331321	610344835	TAIWN-G	COMP	15	0	
STRESS: BALL SHEAR							
CY7C1313V18	4331321	610344833	TAIWN-G	COMP	48	0	
STRESS: BOND PULL							
CY7C1313V18	4331321	610344833	TAIWN-G	COMP	48	0	
STRESS: DIE SHEAR							
CY7C1313V18	4331321	610344833	TAIWN-G	COMP	15	0	
STRESS: EXTERNAL VISUAL							
CY7C1313V18	4331321	610344833	TAIWN-G	COMP	15	0	
STRESS: INTERNAL VISUAL							
CY7C1313V18	4331321	610344833	TAIWN-G	COMP	5	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C1313V18	4331321	610344833	TAIWN-G	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V							
CY7C1313V18	4331321	610344833	TAIWN-G	COMP	9	0	
STRESS: HI-ACCEL SATURATION TEST, 130C, 85%RH, 1.98V, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1313V18	4331321	610344833	TAIWN-G	128	48	0	
STRESS: HIGH TEMPERATURE STORAGE, 150C, no bias							
CY7C1313V18	4331321	610344833	TAIWN-G	500	48	0	
CY7C1313V18	4331321	610344833	TAIWN-G	100	48	0	
STRESS: PHYSICAL DIMENSIONS							
CY7C1313V18	4331321	610344833	TAIWN-G	COMP	5	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1313V18	4331321	610344833	TAIWN-G	168	48	0	
STRESS: THERMAL SHOCK							
CY7C1313V18	4331321	610344833	TAIWN-G	200	48	0	

Reliability Test Data

QTP #: 034209

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: TC COND. C -65C TO 150C, PRECONDITION 192 HRS 30C/60%RH, MSL3							
CY7C1313V18	4331321	610344833	TAIWN-G	300	48	0	
CY7C1313V18	4331321	610344833	TAIWN-G	500	48	0	
CY7C1313V18	4331321	610344834	TAIWN-G	300	48	0	
CY7C1313V18	4331321	610344834	TAIWN-G	500	48	0	
CY7C1313V18	4331321	610344835	TAIWN-G	300	48	0	
CY7C1313V18	4331321	610344835	TAIWN-G	500	48	0	
STRESS: X-RAY							
CY7C1313V18	4331321	610344833	TAIWN-G	COMP	76	0	