

# Cypress Semiconductor Product Qualification Report

QTP# 042505 VERSION 2.0  
April 2006

<b>S4AD-5 Technology, Fab 2</b>	
<b>PSoC Mixed Signal Array (Neutron Product) Family</b>	
<b>CY8C21234 CY8C21334 CY8C21434 CY8C21534 CY8C21634</b>	<b>PSoC™ Mixed Signal Array with On-Chip Controller</b>

## CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

Sabbas Daniel  
VP Quality Engineering  
(408) 943-2685

Fredrick Whitwer  
Principal Reliability Engineer  
(408) 943-2722

### PRODUCT QUALIFICATION HISTORY

<b>Qual Report</b>	<b>Description of Qualification Purpose</b>	<b>Date Comp</b>
010702	New Technology S4AD-5 / New Product, Programmable Clock Generator, CY2414ZC, its product family and bond option.	Apr 01
042505	PSoC 8C21001A Neutron Product Family on SONOS S4AD-5 Technology, Fab2	Dec 04

<b>PRODUCT DESCRIPTION (for qualification)</b>	
Qualification Purpose: Qualify New Device PSoC 8C21001A Neutron Product Family on S4AD-5 Technology, Fab2	
Marketing Part #:	CY8C21234, CY8C21334, CY8C21434, CY8C21534, CY8C21634
Device Description:	3.3V and 5V Industrial 24MHz Programmable System on Chip available in 16-Lead SOIC, 20-Lead SSOP and 32 MLF packages
Cypress Division:	Cypress Semiconductor Corporation – Consumer & Computation Division
Overall Die (or Mask) REV Level (pre-requisite for qualification):	Rev. A
What ID markings on Die:	8C21001A

<b>TECHNOLOGY/FAB PROCESS DESCRIPTION S4AD-5</b>			
Number of Metal Layers:	2	Metal Composition:	Metal 1: 500A Ti/6,000A Al 0.5% Cu /1,200A TiW Metal 2: 500A Ti/8,000A Al 0.5% Cu/300A TiW
Passivation Type and Materials:	3,000A TEOs / 6,000A Si <sub>3</sub> N <sub>4</sub>		
Free Phosphorus contents in top glass layer (%):	0%		
Number of Transistors in Device:	100,000		
Number of Gates in Device	10,000		
Generic Process Technology/Design Rule (μ-drawn):	Single Poly, Double Metal, 0.35 μm		
Gate Oxide Material/Thickness (MOS):	SiO <sub>2</sub> / 110A		
Name/Location of Die Fab (prime) Facility:	Cypress Semiconductor - Round Rock, TX		
Die Fab Line ID/Wafer Process ID:	Fab2, S4AD-5 CTI, SONOS		

**PACKAGE AVAILABILITY**

<b>PACKAGE</b>	<b>ASSEMBLY SITE FACILITY</b>
<b>16-Lead SOIC</b>	<b>OSE Taiwan (TAIWN-T)</b>
<b>20-Lead SSOP</b>	<b>Cypress Philippines (CML-RA)</b>
<b>32-Lead MLF</b>	<b>Amkor-Seoul Korea (SEOL-L)</b>

**Note:** Package Qualification details upon request.

<b>MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION</b>	
<b>Package Designation:</b>	SP20
<b>Package Outline, Type, or Name:</b>	20-Lead Shrunken Small Outline Package (SSOP)
<b>Mold Compound Name/Manufacturer:</b>	Hitachi CEL9220HF
<b>Mold Compound Flammability Rating:</b>	V-O per UL94
<b>Oxygen Rating Index:</b>	>28%
<b>Lead Frame Material:</b>	Copper
<b>Lead Finish, Composition / Thickness:</b>	100% Pure Tin
<b>Die Backside Preparation Method/Metallization:</b>	Backgrind
<b>Die Separation Method:</b>	100% Saw
<b>Die Attach Supplier:</b>	Ablestik
<b>Die Attach Material:</b>	8340
<b>Die Attach Method:</b>	Dispensing
<b>Bond Diagram Designation:</b>	10-06096
<b>Wire Bond Method:</b>	Thermosonic
<b>Wire Material/Size:</b>	Au, 1.0mil
<b>Thermal Resistance Theta JA °C/W:</b>	123°C/W
<b>Package Cross Section Yes/No:</b>	No
<b>Assembly Process Flow:</b>	49-35032
<b>Name/Location of Assembly (prime) facility:</b>	OSE Taiwan (TAIWN-T) (20 SSOP)

<b>ELECTRICAL TEST / FINISH DESCRIPTION</b>	
<b>Test Location:</b>	CML-R
<b>Fault Coverage:</b>	100%

**Note:** Please contact a Cypress Representative for other packages availability.

**RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT**

<b>Stress/Test</b>	<b>Test Condition (Temp/Bias)</b>	<b>Result P/F</b>
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc Max=3.8V, 150°C Dynamic Operating Condition, Vcc Max=5.5V, 125°C	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc Max=3.8V, 150°C	P
High Accelerated Saturation Test (HAST)	130°C, 3.63V, 85%RH Precondition: JESD22 Moisture Sensitivity Level 1  168 Hrs, 85C/85%RH+3IR-Reflow, 235°C+0, -5°C	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity Level 1  168 Hrs, 85C/85%RH+3IR-Reflow, 235°C+0, -5°C Precondition: JESD22 Moisture Sensitivity Level 1  168 Hrs, 85C/85%RH+3IR-Reflow, <b>260°C</b> +0, -5°C	P
Pressure Cooker	121°C, 100%RH Precondition: JESD22 Moisture Sensitivity Level 1  168 Hrs, 85C/85%RH+3IR-Reflow, 235°C+0, -5°C Precondition: JESD22 Moisture Sensitivity Level 1  168 Hrs, 85C/85%RH+3IR-Reflow, <b>260°C</b> +0, -5°C	P
Data Retention	150°C ± 5°C No Bias	P
High Temperature Steady State life	150°C, 3.63V, Vcc Max	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V JESD22, Method A114-B	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,000V/2,200V MIL-STD-883, Method 3015.7	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V Cypress Spec. 25-00020	P
Endurance Test	MIL-STD-883, Method 883-1033	P
Age Bond Strength	200C, 4hrs MIL-STD-883, Method 883-2011	P
Current Density	Cypress Spec 22-00029	P
Low Temperature Operating Life	-30C, 4.3V, 8MHZ	P
SEM Analysis	MIL-STD-883, Method 883-2018-2	P
Acoustic Microscopy	Spec. 25-00104	P
Dynamic Latch up	Cypress Spec. 01-00081	P
Latch up Sensitivity	125C, ± 300mA In accordance with JEDEC 17. Cypress Spec. 01-00081	P

### RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal <sup>3</sup> A.F	Failure Rate
High Temperature Operating Life Early Failure Rate <sup>1</sup>	1,007 Devices	0	N/A	N/A	0 PPM
High Temperature Operating Life <sup>1,2</sup> Long Term Failure Rate	180,000 DHRs	0	0.7	170	30 FIT

<sup>1</sup> Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.

<sup>2</sup> Chi-squared 60% estimations used to calculate the failure rate.

<sup>3</sup> Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp \left[ \frac{E_A}{k} \left[ \frac{1}{T_2} - \frac{1}{T_1} \right] \right]$$

Where:

$E_A$  = The Activation Energy of the defect mechanism.

$k$  = Boltzmann's constant =  $8.62 \times 10^{-5}$  eV/Kelvin.

$T_1$  is the junction temperature of the device under stress and  $T_2$  is the junction temperature of the device at use conditions.

## Reliability Test Data

QTP #: 010702

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
<b>STRESS: ACOUSTIC, MSL1</b>							
CY2414ZC (7C841400A)	2101502	610106170/1/2	TAIWN-T	COMP	15	0	
CY2414ZC (7C841400A)	2052404	610106173/4/5	TAIWN-T	COMP	15	0	
CY2414ZC (7C841400A)	2103764	610106176/7/8	TAIWN-T	COMP	15	0	
<b>STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (150C, 3.8V, Vcc Max)</b>							
CY2414ZC (7C841400A)	2101502	610106170/1/2	TAIWN-T	48	1005	0	
CY2414ZC (7C841400A)	2052404	610106173/4/5	TAIWN-T	48	1004	1	NON VISUAL
CY2414ZC (7C841400A)	2103764	610106176/7/8	TAIWN-T	48	1005	0	
<b>STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (150C, 3.8V, Vcc Max)</b>							
CY2414ZC (7C841400A)	2101502	610106170/1/2	TAIWN-T	80	120	0	
CY2414ZC (7C841400A)	2101502	610106170/1/2	TAIWN-T	500	120	0	
CY2414ZC (7C841400A)	2052404	610106173/4/5	TAIWN-T	80	120	0	
CY2414ZC (7C841400A)	2052404	610106173/4/5	TAIWN-T	500	120	0	
CY2414ZC (7C841400A)	2103764	610106176/7/8	TAIWN-T	80	120	0	
CY2414ZC (7C841400A)	2103764	610106176/7/8	TAIWN-T	500	120	0	
<b>STRESS: AGE BOND STRENGTH</b>							
CY2414ZC (7C841400A)	2101502	610106170/1/2	TAIWN-T	COMP	15	0	
CY2414ZC (7C841400A)	2052404	610106173/4/5	TAIWN-T	COMP	15	0	
CY2414ZC (7C841400A)	2103764	610106176/7/8	TAIWN-T	COMP	15	0	
<b>STRESS: DYNAMIC LATCH-UP TESTING (11.5V)</b>							
CY2414ZC (7C841400A)	2101502	610106170/1/2	TAIWN-T	COMP	3	0	
<b>STRESS: LOW TEMPERATURE OPERATING LIFE (-30C, 4.3V)</b>							
CY2414ZC (7C841400A)	2101502	610106170/1/2	TAIWN-T	500	48	0	
<b>STRESS: HI-ACCEL SATURATION TEST (130C, 85%RH, 3.63V), PRE CONDITION 168 HR 85C/85%RH (MSL1)</b>							
CY2414ZC (7C841400A)	2101502	610106170/1/2	TAIWN-T	128	50	0	
CY2414ZC (7C841400A)	2101502	610106170/1/2	TAIWN-T	256	50	0	
CY2414ZC (7C841400A)	2052404	610106173/4/5	TAIWN-T	128	48	0	
CY2414ZC (7C841400A)	2103764	610106176/7/8	TAIWN-T	128	48	0	

## Reliability Test Data

QTP #: 010702

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
<b>STRESS: ESD-CHARGE DEVICE MODEL (500V)</b>							
CY2414ZC (7C841400A)	2101502	610106170/1/2	TAIWN-T	COMP	9	0	
CY2414ZC (7C841400A)	2052404	610106173/4/5	TAIWN-T	COMP	9	0	
CY2414ZC (7C841400A)	2103764	610106176/7/8	TAIWN-T	COMP	9	0	
<b>STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015 (2,200V)</b>							
CY2414ZC (7C841400A)	2101502	610106170/1/2	TAIWN-T	COMP	9	0	
CY2414ZC (7C841400A)	2052404	610106173/4/5	TAIWN-T	COMP	9	0	
<b>STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015 (2,000V)</b>							
CY2414ZC (7C841400A)	2103764	610106177	TAIWN-T	COMP	10	0	
<b>STRESS: STATIC LATCH-UP TESTING (125C, 10V, ±300mA)</b>							
CY2414ZC (7C841400A)	2101502	610106170/1/2	TAIWN-T	COMP	3	0	
CY2414ZC (7C841400A)	2052404	610106173/4/5	TAIWN-T	COMP	3	0	
CY2414ZC (7C841400A)	2103764	610106176/7/8	TAIWN-T	COMP	3	0	
<b>STRESS: HIGH TEMP STEADY STATE LIFE TEST (150C, 3.63V)</b>							
CY2414ZC (7C841400A)	2101502	610106170/1/2	TAIWN-T	80	80	0	
CY2414ZC (7C841400A)	2101502	610106170/1/2	TAIWN-T	168	80	0	
<b>STRESS: ENDURANCE TEST</b>							
CY2414ZC (7C841400A)	2101502	610106170/1/2	TAIWN-T	COMP	45	0	
<b>STRESS: DATA RETENTION, PLASTIC, 150C</b>							
CY2414ZC (7C841400A)	2101502	610106170/1/2	TAIWN-T	168	80	0	
CY2414ZC (7C841400A)	2101502	610106170/1/2	TAIWN-T	552	80	0	
CY2414ZC (7C841400A)	2052404	610106173/4/5	TAIWN-T	168	80	0	
CY2414ZC (7C841400A)	2052404	610106173/4/5	TAIWN-T	552	80	0	
CY2414ZC (7C841400A)	2103764	610106176/7/8	TAIWN-T	168	80	0	
CY2414ZC (7C841400A)	2103764	610106176/7/8	TAIWN-T	552	80	0	
<b>STRESS: PRESSURE COOKER TEST (121C, 100%RH), PRE CONDITION 168 HR 85C/85%RH (MSL1)</b>							
CY2414ZC (7C841400A)	2101502	610106170/1/2	TAIWN-T	168	50	0	
CY2414ZC (7C841400A)	2052404	610106173/4/5	TAIWN-T	168	49	0	
CY2414ZC (7C841400A)	2103764	610106176/7/8	TAIWN-T	168	51	0	



## Reliability Test Data

QTP #: 010702

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
<b>STRESS: TC COND. C -65C TO 150C, PRECONDITION 168 HRS 85C/85%RH (MSL1)</b>							
CY2414ZC (7C841400A)	2101502	610106170/1/2	TAIWN-T	300	50	0	
CY2414ZC (7C841400A)	2101502	610106170/1/2	TAIWN-T	500	50	0	
CY2414ZC (7C841400A)	2101502	610106170/1/2	TAIWN-T	1000	50	0	
CY2414ZC (7C841400A)	2052404	610106173/4/5	TAIWN-T	300	50	0	
CY2414ZC (7C841400A)	2052404	610106173/4/5	TAIWN-T	500	50	0	
CY2414ZC (7C841400A)	2052404	610106173/4/5	TAIWN-T	1000	50	0	
CY2414ZC (7C841400A)	2103764	610106176/7/8	TAIWN-T	300	50	0	
CY2414ZC (7C841400A)	2103764	610106176/7/8	TAIWN-T	500	50	0	
CY2414ZC (7C841400A)	2103764	610106176/7/8	TAIWN-T	1000	49	0	

## Reliability Test Data

QTP #: 042505

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
<b>STRESS: ESD-CHARGE DEVICE MODEL, (500V)</b>							
CY8C21334 (8C21334A)	2425372	610443723	TAIWN-T	COMP	9	0	
<b>STRESS: ESD-HUMAN BODY CIRCUIT PER JESD22, METHOD A114-B, (2,200V)</b>							
CY8C21334 (8C21334A)	2425372	610443723	TAIWN-T	COMP	9	0	
<b>STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, (2,200V)</b>							
CY8C21334 (8C21334A)	2425372	610443723	TAIWN-T	COMP	3	0	
<b>STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (125C, 5.5V, Vcc Max)</b>							
CY8C21334 (8C21334A)	2427548	610458304N	TAIWN-T	96	1007	0	
<b>STRESS: PRESSURE COOKER TEST (121C, 100%RH), PRE CONDITION 168 HR 85C/85%RH (MSL1)</b>							
CY8C21334 (8C21334A)	2425372	610443723	TAIWN-T	168	45	0	
CY8C21334 (8C21334A)	2425372	610443723	TAIWN-T	288	45	0	
<b>STRESS: STATIC LATCH-UP TESTING (125C, 11V, ±300mA)</b>							
CY8C21334 (8C21334A)	2425372	610443723	TAIWN-T	COMP	3	0	
<b>STRESS: TC COND. C -65C TO 150C, PRECONDITION 168 HRS 85C/85%RH (MSL1)</b>							
CY8C21334 (8C21334A)	2425372	610443723	TAIWN-T	300	45	0	
CY8C21334 (8C21334A)	2425372	610443723	TAIWN-T	500	45	0	