Cypress Semiconductor
Product Qualification Report

QTP# 002104 VERSION 2.0
October, 2003

EnCoRe™ USB P26TLM Technology, Fab 2-CTI	
CY7C63221A/ CY7C63231A	Low Speed USB Peripheral Controller

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PRODUCT QUALIFICATION HISTORY

Qual Report	Description of Qualification Purpose	Date Comp
99273	New P26 with TML Technology Qualification	Oct 99
002104	New CY7C63221A/31A USB product Qualification, P26 with TML Technology	Apr 00

PRODUCT DESCRIPTION (for qualification)		
Qualification Purpose: To qualify CY7C63221A/31A in qualified P26TLM Technology, Fab 2..		
Marketing Part #:	CY7C63221A/CY7C63231A	
Device Description:	3.3V, Commercial, available in 16-lead PDIP and 18-lead PDIP/SOIC Package.	
Cypress Division:	Cypress Semiconductor Corporation – Interface Product Division (IPD)	
Overall Die (or Mask) REV:		Rev. A
What ID markings on Die:	7C6320A	

TECHNOLOGY/FAB PROCESS DESCRIPTION			
Number of Metal Layers:	3	Metal Composition:	Metal 1: 6000Å Al, 1200 Å TiW Metal 2: 1500Å TiW, 9000Å Al, 320Å TiW Metal 3: 320 ÅTiW/10000 ÅAl/1500Å TiW
Generic Process Technology/Design Rule (µ-drawn):	Triple Metal / 0.65µm		
Gate Oxide Material/Thickness (MOS):	SiO_2 / 65 Å		
Name/Location of Die Fab (prime) Facility:	Cypress Semiconductor - Round Rock, TX (Fab2)		
Die Fab Line ID/Wafer Process ID:	Fab 2/ P26TLM		

PACKAGE AVAILABILITY

PACKAGE TYPE	ASSEMBLY SITE FACILITY
18-lead SOIC	PHIL-M
16/18-lead PDIP	INDNS-O / ALPHA-X

Note: Package Qualification details upon request

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	P183A
Package Outline, Type, or Name:	18-lead, Plastic Dual-In Line Package (PDIP)
Mold Compound Name/Manufacturer:	Sumitomo EME-6300
Mold Compound Flammability Rating:	V-O per UL 94
Oxygen Rating Index:	>28%
Lead Frame Designation:	P
Lead Frame Material:	Copper
Lead Finish, Composition / Thickness:	Solder Plated, 85%Sn, 15%Pb
Die Backside Preparation Method/Metallization:	N/A
Die Separation Method:	Wafer Saw
Die Attach Supplier:	Ablestik
Die Attach Material:	Ablestik 8361
Bond Diagram Designation	10-03825
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au, 1.0um
Thermal Resistance Theta JA °C/W:	80
Package Cross Section Yes/No:	N/A
Assembly Process Flow:	49-70027M
Name/Location of Assembly (prime) facility:	OMEDATA (INDNS-O)

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	OMEDATA (INDNS-O)
Fault Coverage:	100%

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENTS

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc = 5.75V, 150°C	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc = 5.75V, 150°C	P
Extended Dynamic Burn-in	Dynamic Operating Condition, Vcc = 5.75V, 150°C	P
High Accelerated Saturation Test (HAST)	130°C/140°/5.5V, 85%RH Precondition: JESD22 Moisture Sensitivity Level 1 168 Hrs, 85°C/85%RH+3IR-Reflow, 220°C+5, -0°C	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity Level 1 168 hrs, 85°C/85%RH+3IR-Reflow, 220°C+5, -0°C	P
Electrostatic Discharge Human Body Model (ESD-HBM)	MIL-STD-883, Method 3015.7 (2,200V)	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	Cypress Spec. 25-00020 (1,000V)	P
High Temperature Storage	16°5C, No Bias	P
Static Latchup Sensitivity	In accordance with JEDEC 17. Cypress Spec. 01-00081 (±300mA)	P
Pressure Cooker	Cypress Spec. 25-00047, 121°C/100%RH Precondition: JESD22 Moisture Sensitivity Level 1 168 hrs, 85°C/85%RH+3IR-Reflow, 220°C+5, -0°C	P
Age Bond	MIL-STD-883, Method 2011	P
Acoustic Microscopy	Cypress Spec 25-000104	P
SEM	MIL-STD-883, Method 2018-2	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Acceleration Factor[3]	Failure Rate[4]
High Temperature Operating Life Early Failure Rate	4,078	0	N/A	N/A	0 PPM
High Temperature Operating Life[1,2] Long Term Failure Rate	248,100 DHRs	0	0.7	170	22 FIT

[1] Assuming an ambient temperature of 150°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate.
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

[4] **EFR and LFR based on QTP 99273 and 002104**

Reliability Test Data

QTP #: 002104

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERTING LIFE - EARLY FAILURE RATE (150C, 5.75V, VCC MAX)							
CY7C63231A-PC	2031881	*510010227/8*	INDNS-O	48	497	0	
CY7C63231A-PC	2031881	*510010227/8*	INDNS-O	48	503	0	
STRESS: HIGH TEMP DYNAMIC OPERTING LIFE-LATENT FAILURE RATE (150C, 5.75V, Vcc Max)							
CY7C63231A-PC	2031881	*510010227/8*	INDNS-O	80	117	0	
CY7C63231A-PC	2031881	*510010227/8*	INDNS-O	500	117	0	
STRESS: PRESSURE COOKER TEST (121C, 100%RH)							
CY7C63231A-PC	2031881	*510010227/8*	INDNS-O	168	46	0	
STRESS: STATIC LATCH-UP TESTING (125C, 11.5V, +/-300mA)							
CY7C63231A-PC	2031881	*510010227/8*	INDNS-O	COMP	3	0	

RELIABILITY TEST DATA

QTP#: 99273

DEVICE	ASSY-LOC	FABLOT#	ASSYLOT#	DURATION	S/S	REJ	FAIL MODE
STRESS: HIGH TEMPERATURE STORAGE -PLASTIC (165C, NO BIAS)							
7C6399AT	CSPI-R	2920309	619918583	168	78	0	
7C6399AT	CSPI-R	2920309	619918583	552	78	0	
7C6399AT	CSPI-R	2931408	619927766	168	81	0	
7C6399AT	CSPI-R	2931408	619927766	552	81	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (150C, 5.75V)							
7C6399AT	INDNS-O	2920309	519911818/19/20	48HRS	978	0	
7C6399AT	CSPI-R	2931408	519915664/5756/	48	1000	0	
7C6399AT	CSPI-R	2920309	619918583	48	1100	0	
STRESS: ESD-CHARGE DEVICE MODEL (1000V)							
7C6399AT	CSPI-R	2920309	619918583	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015 (2200V)							
7C6399AT	CSPI-R	2920309	619918583	COMP	3	0	
STRESS: HI-ACCEL SATURATION TEST (140C/85%RH/5.5V), PRECOND. 168 HRS 85C/85%RH							
7C6399AT	CSPI-R	2920309	619918583	128	50	0	
7C6399AT	CSPI-R	2931408	619927766	128	49	0	
STRESS: HIGH TEMPERATURE STORAGE (165C, NO BIAS)							
7C6399AT	CSPI-R	2920309	619918583	336	46	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (150C, 5.75V)							
7C6399AT	INDNS-O	2920309	519911818/19/20	80	120	0	
7C6399AT	INDNS-O	2920309	519911818/19/20	500	120	0	
7C6399AT	CSPI-R	2931408	519915664/5756/	80	120	0	
STRESS: EXTENDED DYNAMIC BURN-IN (150C, 5.75V)							
7C6399AT	CSPI-R	2920309	619918583	1000	120	0	
STRESS: PRESSURE COOKER TEST (121C, 100%RH)							
7C6399AT	CSPI-R	2920309	619918583	168	47	0	
STRESS: TC COND. C, -65 TO 150C, PRECOND. 168 HRS 85C/85%RH (MSL 1)							
7C6399AT	CSPI-R	2920309	619918583	300	45	0	