

# **Cypress Semiconductor Product Qualification Report**

**QTP# 001205 VERSION 1.3  
May, 2003**

**Low Cost Three-PLL Clock Generator  
CY2081SC/CY2081SL  
TSMC-2A, Taiwan**

**CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:**

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### PRODUCT QUALIFICATION HISTORY

<b>Qual Report</b>	<b>Description of Qualification Purpose</b>	<b>Date Comp</b>
001205	Qualify CY2081SC/CY2081SL in TSMC Fab 2A	Apr 00

<b>PRODUCT DESCRIPTION (for qualification)</b>	
Qualification Purpose: To qualify CY2081SC/CY2081SL in TSMC Fab 2A	
Marketing Part #:	CY2081SC/CY2081SL
Device Description:	3.3V, 5V, available in 8pin SOIC
Cypress Division:	Cypress Semiconductor Corporation - TTD WA Division
Overall Die (or Mask) REV:	D
What ID markings on Die:	7C83002A

<b>TECHNOLOGY/FAB PROCESS DESCRIPTION - L28-TSMC</b>			
Number of Metal Layers:	2	Metal Composition:	Metal 1: Ti 400Å /TiN1,000Å /AlSiCu 4,700Å /TiN 375Å Metal 2: Ti 1,500Å / AlSiCu 8,000Å / TiN 375Å
Passivation Type and Materials:	SiN 3,000Å /SOG 3,150Å /SiN 12,000Å		
Generic Process Technology/Design Rule (μ-drawn):	CMOS, Single Poly, Double Metal /0.65 μm		
Gate Oxide Material/Thickness (MOS):	SiO <sub>2</sub> / 125 Å		
Name/Location of Die Fab (prime) Facility:	TSMC-2A, Taiwan		
Die Fab Line ID/Wafer Process ID:	TSMC-2A /L28-TSMC		

### RELIABILITY TESTS PERFORMED

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc = 5.75V, 150°C	P
Electrostatic Discharge Human Body Model (ESD-HBM)	MIL-STD-883, Method 3015.7	P 3,300V
Electrostatic Discharge Charge Device Model (ESD-CDM)	Cypress Spec. 25-00020	1,000V
Latchup Sensitivity	In accordance with JEDEC 17. Cypress Spec. 01-00081	10.5 V ± 300mA

### RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Acceleration Factor <sup>4</sup>	Failure Rate <sup>5</sup>
High Temperature Operating Life Early Failure Rate <sup>1</sup>	1051	0	N/A	N/A	0 PPM
High Temperature Operating Life <sup>2,3</sup> Long Term Failure Rate	181,660 DHRs	0	0.7	170	30 FIT

<sup>2</sup> Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.

<sup>3</sup> Chi-squared 60% estimations used to calculate the failure rate.

<sup>4</sup> Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp \left[ \frac{E_A}{k} \left[ \frac{1}{T_2} - \frac{1}{T_1} \right] \right]$$

where:

$E_A$  = The Activation Energy of the defect mechanism.

$k$  = Boltzmann's constant =  $8.62 \times 10^{-5}$  eV/Kelvin.

$T_1$  is the junction temperature of the device under stress and  $T_2$  is the junction temperature of the device at use conditions.

<sup>1</sup>Early Term Failure Rate based on QTP #001205.

<sup>5</sup>Long Term Failure Rate based on QTP #99285, L28-TSMC Technology, TSMC-2A qualification.

**RELIABILITY TEST DATA**

**QTP#: 99285<sup>6</sup>**

DEVICE	ASSY-LOC	FABLOT#	ASSYLOT#	DURATION	S/S	REJ	FAIL MODE
STRESS: DATA RETENTION (150C)							
CY2280-OC	CSPI-R	2937109	619927291/2/3	500	85	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (150C, 3.8V)							
CY2280-OC	CSPI-R	2937109	619927291/2/3	48	335	0	
CY2280-OC	CSPI-R	2937190	619928659/60/61	48	234	0	
CY2280-OC	CSPI-R	2937190	619928659/60/61	48	101	0	
CY2280-OC	CSPI-R	2942829	619933793/4/5	48	349	0	
STRESS: ESD-CHARGE DEVICE MODEL (1000V)							
CY2280-OC	CSPI-R	2937109	619927291/2/3	COMP	3	0	
CY2280-OC	CSPI-R	2937190	619928659/60/61	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015 (2,200V)							
CY2280-OC	CSPI-R	2937109	619927291/2/3	COMP	3	0	
CY2280-OC	CSPI-R	2937190	619928659/60/61	COMP	3	0	
STRESS: HI-ACCEL SATURATION TEST (140C/85%RH/3.63V), PRECOND. 168 HRS 85C/85%RH							
CY2280-OC	CSPI-R	2937109	619927291/2/3	S/RE-FLOW	50	0	
CY2280-OC	CSPI-R	2937109	619927291/2/3	128	50	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST (150C, 3.63V)							
CY2280-OC	CSPI-R	2937109	619927291/2/3	80	77	0	
CY2280-OC	CSPI-R	2937109	619927291/2/3	168	77	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (150C, 3.8V)							
CY2280-OC	CSPI-R	2937109	619927291/2/3	80	120	0	
CY2280-OC	CSPI-R	2937109	619927291/2/3	500	120	0	
CY2280-OC	CSPI-R	2937190	619928659/60/61	80	120	0	
CY2280-OC	CSPI-R	2937190	619928659/60/61	500	120	0	
CY2280-OC	CSPI-R	2942829	619933793/4/5	80	125	0	
CY2280-OC	CSPI-R	2942829	619933793/4/5	500	123	0	
STRESS: LOW TEMPERATURE OPERATING LIFE (-30C/8MHZ)							
CY2280-OC	CSPI-R	2937190	619928659/60/61	500	50	0	
STRESS: PRESSURE COOKER TEST, MSL 1 (121C, 100%RH)							
CY2280-OC	CSPI-R	2937109	619927291/2/3	S/RE-FLOW	53	0	
CY2280-OC	CSPI-R	2937109	619927291/2/3	168	53	0	
STRESS: TC COND. C, -65 TO 150C, PRECOND. 168 HRS 85C/85%RH (MSL 1)							
CY2280-OC	CSPI-R	2937109	619927291/2/3	S/RE-FLOW	50	0	
CY2280-OC	CSPI-R	2937109	619927291/2/3	300	50	0	

<sup>6</sup>QTP #99285, L28-TSMC Technology, TSMC-2A qualification.

## Reliability Test Data

QTP #: 001205

<i>Device</i>	<i>Fab Lot #</i>	<i>Assy Lot #</i>	<i>Assy Loc</i>	<i>Duration</i>	<i>Samp</i>	<i>Rej</i>	<i>Failure Mechanism</i>
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**STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (150C, 5.75V,Vcc Max)**

CY2081SL-SC	2949741	610005232/3/4	PHIL-M	48	186	0	
CY2081SL-SC	2949741	610005232/3/4	PHIL-M	48	185	0	
CY2081SL-SC	2949741	610005232/3/4	PHIL-M	48	340	0	
CY2081SL-SC	2949741	610005232/3/4	PHIL-M	48	340	0	

**STRESS: ESD-CHARGE DEVICE MODEL (1,000V)**

CY2081SL-SC	2949741	610005232/3/4	PHIL-M	COMP	3	0	
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**STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015 (3,300V)**

CY2081SL-SC	2949741	610005232/3/4	PHIL-M	COMP	4	0	
CY2081SL-SC	2949741	610005232/3/4	PHIL-M	COMP	3	0	