Cypress Semiconductor
Product Qualification Report

QTP# 013405 VERSION 1.1
May, 2003

Clock Generator **L28 Technology, Fab 2**	
CY5040WAF/ **CY2040***	**32kHz and 24MHz Clock Generator with Precision 32kHz input**

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

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PRODUCT QUALIFICATION HISTORY

Qual Report		Description of Qualification Purpose		Date Comp
97403		New Technology L28/New Device CY227*		Apr 98
005003		New CY5040WAF/ CY2040* device family		Aug 01
013405		3 layer change to enhance		Nov 01

PRODUCT DESCRIPTION (for qualification)			
Qualification Purpose: Qualify 3 layer change to CY20540WAF/CY20240* device family in L28 Technology , Fab 2.			
Marketing Part #:	CY20540WAF/CY20240*		
Device Description:	3.3V, Commercial available via Die sale form and in 16-lead TSSOP/SOIC Package.		
Cypress Division:	Cypress Semiconductor Corporation – Interface Clock Division (ICD) WA		
Overall Die (or Mask) REV Level (pre-requisite for qualification):		Rev. A	
What ID markings on Die:	7C80400A		

TECHNOLOGY/FAB PROCESS DESCRIPTION - L28			
Number of Metal Layers:	2	Metal Composition:	Metal 1: 500A Ti/1,200A TiW/6,000A Al/1,200A TiW Metal 2: 1,500A TiW//10,000A Al/150A Ti
Passivation Type and Materials:		3,000A TEOS + 15,000A Si_2N_4	
Free Phosphorus contents in top glass layer(%):		N/A	
Die Coating(s), if used:		N/A	
Generic Process Technology/Design Rule (μ-drawn):		CMOS, Single Poly, Double Metal /0.65 μm	
Gate Oxide Material/Thickness (MOS):		SiO_2 / 145 A	
Name/Location of Die Fab (prime) Facility:		Cypress Semiconductor - Round Rock, TX	
Die Fab Line ID/Wafer Process ID:		Fab2/L28	

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY FACILITY SITE
16-lead SOIC	**Cypress Philippines (CSPI-R)**
16-lead TSSOP	**OSE Taiwan (TAIWN-T), Cypress Philippines (CSPI-R)**

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	Z1613
Package Outline, Type, or Name:	16-lead TSSOP
Mold Compound Name/Manufacturer:	SHINETSU KMC – 184-2
Mold Compound Flammability Rating:	V-O per UL94
Oxygen Rating Index:	>28%
Lead Frame Material:	Copper
Lead Finish, Composition / Thickness:	Solder Plated, 85%Pb, 15%Sn
Die Backside Preparation Method/Metallization:	Grinding / 10 mils
Die Separation Method:	Diamond wheel Dicing
Die Attach Supplier:	ASM
Die Attach Material:	84-1LMIS
Die Attach Method:	Dispensing
Bond Diagram Designation:	10-04439
Wire Bond Method:	Thermal Ultrasonic
Wire Material/Size:	Au, 1.0mil
Thermal Resistance Theta JA °C/W:	116.8°C/W
Package Cross Section Yes/No:	N/A
Assembly Process Flow:	49-35003
Name/Location of Assembly (prime) facility:	OSE Taiwan (TAIWN-T)

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	OSE Taiwan (TAIWN-T)
Fault Coverage:	100%

Note: Please contact a Cypress Representative for other packages availability.

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENTS

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc = 3.65V, 150C Dynamic Operating Condition, Vcc = 3.8V, 150C	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc = 3.65V, 150°C	P
Read and Record Life Test	Dynamic Operating Condition, Vcc = 3.65V, 150°C	P
High Accelerated Saturation Test (HAST)	140°C, 85%RH, 5.5V Precondition: JESD22 Moisture Sensitivity Level 1 168 Hrs., 85°C/85%RH+3IR-Reflow, 220°C+5, -0°C	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity Level 1 168 Hrs., 85°C/85%RH+3IR-Reflow, 220°C+5, -0°C	P
Cold Life Test	-30°C, 6.5V	P
Age Bond Strength	MIL-STD-883, Method 2011	P
Data Retention-Plastic	165°C, No Bias	P
High Temperature Storage	165°C, No Bias	
Electrostatic Discharge Charge Device Model (ESD-CDM)	Cypress Spec. 25-00020 (500V)	P
Electrostatic Discharge Human Body Model (ESD-HBM)	MIL-STD-883, Method 3015.7 (2,000V)	P
Latchup Sensitivity	±300mA ±200mA In accordance with JEDEC 17. Cypress Spec. 01-00081	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal[3] A.F	Failure Rate[4]
High Temperature Operating Life Early Failure Rate	1,850 Devices	0	N/A	N/A	0 PPM
High Temperature Operating Life[1,2] Long Term Failure Rate	173,,900 DHRs	0	0 .7	170	31 FIT

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate.
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

[4] EFR Failure Rate based on QTP #005003 and QTP #97403.
[4] LFR FIT Rate based on QTP #97403.

RELIABILITY TEST DATA

QTP 97403

DEVICE	ASSY-LOC	FABLOT#	ASSYLOT#	DURATION	S/S	REJ	FAIL MODE
STRESS: DATA RETENTION (165C, NO BIAS)							
CY2273APVC(7C82731A)	CSPI-R	2732995	619708289/319	168	78	0	
CY2273APVC(7C82731A)	CSPI-R	2732995	619708289/319	552	78	0	
CY2273APVC(7C82731A)	CSPI-R	2735423	619709731	168	78	0	
CY2273APVC(7C82731A)	CSPI-R	2735423	619709731	552	78	0	
CY2273APVC(7C82731A)	CSPI-R	2734307	619709732	168	78	0	
CY2273APVC(7C82731A)	CSPI-R	2734307	619709732	552	78	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (150C, 3.65V)							
CY2273APVC(7C82731A)	CSPI-R	2732995	619708289/319	48	180	0	
CY2273APVC(7C82731A)	CSPI-R	2735423	619709731	48	340	0	
CY2273APVC(7C82731A)	CSPI-R	2734307	619709732	48	330	0	
STRESS: ESD-CHARGE DEVICE MODEL, 2000V							
CY2273APVC(7C82731A)	CSPI-R	2732995	619708289/319	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 4000V							
CY2273APVC(7C82731A)	CSPI-R	2732995	619708289/319	COMP	3	0	
STRESS: STRESS: STATIC LATCH-UP TESTING (125C, 10V, ±200mA)							
CY2273APVC(7C82731A)	CSPI-R	2732995	619708289/319	COMP	3	0	
STRESS: HI-ACCEL SATURATION TEST (140C, 3.63V, 85%RH), PRECOND. 168 HRS 85C/85%RH							
CY2273APVC(7C82731A)	CSPI-R	2732995	619708289/319	128	44	0	
CY2273APVC(7C82731A)	CSPI-R	2732995	619708289/319	256	44	0	
CY2273APVC(7C82731A)	CSPI-R	2734307	619709732	128	45	0	
STRESS: HIGH TEMPERATURE STORAGE (165C, NO BIAS)							
CY2273APVC(7C82731A)	CSPI-R	2732995	619708289/319	336	45	0	
CY2273APVC(7C82731A)	CSPI-R	2732995	619708289/319	500	45	0	
CY2273APVC(7C82731A)	CSPI-R	2732995	619708289/319	1000	45	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (150C, 3.65V)							
CY2273APVC(7C82731A)	CSPI-R	2732995	619708289/319	80	116	0	
CY2273APVC(7C82731A)	CSPI-R	2732995	619708289/319	500	116	0	
CY2273APVC(7C82731A)	CSPI-R	2735423	619709731	80	120	0	
CY2273APVC(7C82731A)	CSPI-R	2735423	619709731	500	116	0	
CY2273APVC(7C82731A)	CSPI-R	2734307	619709732	80	116	0	
CY2273APVC(7C82731A)	CSPI-R	2734307	619709732	500	115	0	
STRESS: COLD LIFE TEST (-30C, 6.5V)							
CY2273APVC(7C82731A)	CSPI-R	2732995	619708289/319	500	45	0	
CY2273APVC(7C82731A)	CSPI-R	2732995	619708289/319	1000	44	0	

RELIABILITY TEST DATA

QTP 97403

DEVICE	ASSY-LOC	FABLOT#	ASSYLOT#	DURATION	S/S	REJ	FAIL MODE
STRESS: READ & RECORD LIFE TEST (150C, 3.65V)							
CY2273APVC(7C82731A)	CSPI-R	2734307	619709732	48	10	0	
CY2273APVC(7C82731A)	CSPI-R	2734307	619709732	80	10	0	
CY2273APVC(7C82731A)	CSPI-R	2734307	619709732	500	10	0	
STRESS: TC COND. C, -65 TO 150C, PRECOND. 168 HRS 85C/85%RH							
CY2273APVC(7C82731A)	CSPI-R	2732995	619708289/319	300	45	0	
CY2273APVC(7C82731A)	CSPI-R	2732995	619708289/319	1000	45	0	
CY2273APVC(7C82731A)	CSPI-R	2735423	619709731	300	48	0	
CY2273APVC(7C82731A)	CSPI-R	2735423	619709731	1000	48	0	
CY2273APVC(7C82731A)	CSPI-R	2734307	619709732	300	47	0	
CY2273APVC(7C82731A)	CSPI-R	2734307	619709732	1000	47	0	

Reliability Test Data

QTP #: 005003

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (150C, 3.8V, Vcc Max)							
CY5040-SC (7C80400A)	2104872	*61011457*	CSPI-R	48	1000	0	
STRESS: ESD-CHARGE DEVICE MODEL (500V)							
CY5040-SC (7C80400A)	2104872	*61011457*	CSPI-R	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015 (2,200V)							
CY5040-SC (7C80400A)	2104872	*61011457*	CSPI-R	COMP	9	0	
STRESS: STATIC LATCH-UP TESTING (125C, 10V, +/-300mA)							
CY5040-SC (7C80400A)	2104872	*61011457*	CSPI-R	COMP	3	0	

Reliability Test Data

QTP #: 013405

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-CHARGE DEVICE MODEL (500V)							
CY2040ZC (7C80400A)	2135544	*610133865/7/9*	CSPI-R	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015 (2,000V)							
CY2040ZC (7C80400A)	2135544	*610133865/7/9*	CSPI-R	COMP	9	0	
STRESS: STATIC LATCH-UP TESTING (125C, 10V, +/-300mA)							
CY2040ZC (7C80400A)	2135544	*610133865/7/9*	CSPI-R	COMP	3	0	