Cypress Semiconductor
Product Qualification Report

QTP# 004504 VERSION 1.2
May, 2003

Unidirectional/Bidirectional/Tri Bus Synchronous FIFO **R52FFD-3 Technology, Fab 4**	
CY7C43643AV	1K x 36
CY7C43663AV	4K x 36
CY7C43683AV	16K x 36
CY7C43642AV/CY7C43644AV	1K x 36 x 2
CY7C43662AV/CY7C43664AV	4K x 36 x 2
CY7C43682AV/CY7C43684AV	16K x 36x 2
CY7C43646AV	1K x 36/ x 18 x 2
CY7C43666AV	4K x 36/ x 18 x 2
CY7C43686AV	16K x 36/ x 18 x 2

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

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PRODUCT QUALIFICATION HISTORY

Qual Report		Description of Qualification Purpose		Date Comp
004504		New Device, Unidirectional/Bidirectional/Tri Bus Synchronous FIFO CY7C43684AV and its FIFO Family, R52FFD-3		June 01
011105		UV Process change for R52FFD-3 to enhance functionality		June 01

PRODUCT DESCRIPTION (for qualification)		
Qualification Purpose: Qualify New Device CY7C43684AV and its FIFO family in R52FFD-3 Technology, Fab4.		
Marketing Part #:	CY7C43644AV, CY7C43664AV,CY7C43684AV	
Device Description:	3.3V, Commercial and Industrial, available in 120/128-pin TQFP package	
Cypress Division:	Cypress Semiconductor Corporation – Data Com Division (DCD)	
Overall Die (or Mask) REV:		Rev. B
What ID markings on Die:	7C43384B	

TECHNOLOGY/FAB PROCESS DESCRIPTION			
Number of Metal Layers:	2	Metal Composition:	Metal 1: 500Å TiW/6,000Å Al-0.5%Cu/300Å TiW Metal 2: 300Å Ti/8,000Å Al-0.5%Cu/300Å TiW
Passivation Type and Materials:		1,000 Å Oxide / 9,000A Nitride	
Free Phosphorus contents in top glass layer(%):		0%	
Die Coating(s), if used:		N/A	
Number of Transistors:		6,417,000	
Number of Gates:		16,000	
Generic Process Technology/Design Rule (μ-drawn):		CMOS, Double Metal, 0.25 μm	
Gate Oxide Material/Thickness (MOS):		SiO_2 55Å	
Name/Location of Die Fab (prime) Facility:		Cypress Semiconductor – Bloomington, MN	
Die Fab Line ID/Wafer Process ID:		Fab4/R52FFD-3	

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY FACILITY SITE
128-pins TQFP	**TAIWN-G**

Note: Package Qualification details upon request.

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	A128
Package Outline, Type, or Name:	128-pin Thin Quad Flat Pack (TQFP)
Mold Compound Name/Manufacturer:	Sumitomo EME 7320A
Mold Compound Flammability Rating:	V-O per UL 94
Oxygen Rating Index:	>28%
Substrate Material:	Copper
Lead Finish, Composition / Thickness:	Solder Plated, 85%Sn, 15%Pb
Die Backside Preparation Method/Metallization:	N/A
Die Separation Method:	Wafer Saw
Die Attach Supplier:	Ablestik
Die Attach Material:	8361H
Die Attach Method	Epoxy
Bond Diagram Designation	10-03658
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au,1.0um
Thermal Resistance Theta JA °C/W at 0 Airflow:	40°C/W
Package Cross Section Yes/No:	N/A
Assembly Process Flow:	49-41004
Name/Location of Assembly (prime) facility:	ASE Taiwan (TAIWN-G)

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	Cypress, USA, CSPI-R
Fault Coverage:	100%

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENTS

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure	Dynamic Operating Condition, Vcc = 3.8V, 125°C	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc = 3.8V, 125°C	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity Level 3 192 Hrs., 30°C/60%RH+3IR-Reflow, 220°C+5, -0°C	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V Cypress Spec. 25-00020	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V MIL-STD-883, Method 3015.7	P
Acoustic Microscopy, Level 3	Cypress Spec. 25-00104	P
Latchup Sensitivity	125ºC, 7.5V, ± 300mA In accordance with JEDEC 17. Cypress Spec. 01-00081	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Acceleration Factor[4]	Failure Rate[5]
High Temperature Operating Life Early Failure Rate[1]	4,072	1	N/A	N/A	246 PPM
High Temperature Operating Life Long Term Failure Rate[2,,3]	554,872 HRs	0	0.7	55	30 FIT

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[1] A production burn-in of 12 Hrs at 125°C, 4.0V is required for the product.
[2] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[3] Chi-squared 60% estimations used to calculate the failure rate.
[4] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

[5] **EFR and LFR FIT Rate based on QTP #004504 and 011105.**

Reliability Test Data

QTP #: 004504

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (125C, 4.0V)							
CY7C43684AV (7C43384B)	4046388	*610100750*	TAIWN-G	84	162	0	
CY7C43684AV (7C43384B)	4046388	*610100750N1*	TAIWN-G	84	469	0	
CY7C43684AV (7C43384B)	4046388	*610101253*	TAIWN-G	84	479	0	
CY7C43684AV (7C43384B)	4046388	*610103325*	TAIWN-G	84	823	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (125C, 3.8V, Vcc Max)							
CY7C43684AV (7C43384B)	4046388	*610100750*	TAIWN-G	168	55	0	
CY7C43684AV (7C43384B)	4046388	*610100750*	TAIWN-G	1000	510		
CY7C43684AV (7C43384B)	4046388	*610101253*	TAIWN-G	168	55	0	
CY7C43684AV (7C43384B)	4046388	*610101253*	TAIWN-G	1000	520		
CY7C43684AV (7C43384B)	4046388	*610103325*	TAIWN-G	168	110	0	
CY7C43684AV (7C43384B)	4046388	*610103325*	TAIWN-G	1000	102	0	
STRESS: ESD-CHARGE DEVICE MODEL (500V)							
CY7C43684AV-AC (7C43384B)	4046388	*610101253*	TAIWN-G	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015 (2,200V)							
CY7C43684AV-AC (7C43384B)	4046388	*610101253*	TAIWN-G	COMP	9	0	
STRESS: STATIC LATCH-UP TESTING (125C, 7.5V, +/300mA)							
CY7C43684AV-AC (7C43384B)	4046388	*610101253*	TAIWN-G	COMP	3	0	
STRESS: ACOUSTIC)							
CY7C43684AV-AC (7C43384B)	4046388	*610101253*	TAIWN-G	COMP	15	0	
STRESS: TC COND. C -65C TO 150C, PRECONDITION 192 HRS 30C/60%RH (MSL3)							
CY7C43684AV-AC (7C43384B)	4046388	*610101253*	TAIWN-G	300	47	0	

Reliability Test Data

QTP #: 011105

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (125C, 3.8V, Vcc Max)							
CY7C43684AV-AC (7C43384B)	4051483	*610106983N1*	TAIWN-G	96	1027	0	
CY7C43684AV-AC (7C43384B)	4103662	*610111052*	TAIWN-G	96	1112	1	SCRATCH ON METAL BUS LINE
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (125C, 3.8V, Vcc Max)							
CY7C43684AV-AC (7C43384B)	4051483	*610106983N1*	TAIWN-G	168	179	0	
CY7C43684AV-AC (7C43384B)	4051483	*610106983N1*	TAIWN-G	1000	171	0	
CY7C43684AV-AC (7C43384B)	4103662	*610111052*	TAIWN-G	168	180	0	
CY7C43684AV-AC (7C43384B)	4103662	*610111052*	TAIWN-G	1000	174	0	
****STRESS: TC COND. C -65C TO 150C***							
CY7C43684AV-AC (7C43384B)	4051483	*610106983N1*	TAIWN-G	300	50	0	
CY7C43684AV-AC (7C43384B)	4103662	610111052	TAIWN-G	300	50	0	

***Note: No Precondition required**