Cypress Semiconductor
Product Qualification Report

QTP# 004405 VERSION 1.2
December, 2002

Micro Power Asynchronous R52LD-5R Technology Fab 4 Cypress	
CY62148B	**512K x 8 Static RAM**

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

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PRODUCT QUALIFICATION HISTORY

Qual Report	Description of Qualification Purpose	Date Comp
99396	New R52LD-5R Technology Derivative /New CY62128B,1Meg SRAM Product	Sep 00
004405	New CY62148B, 4Meg Product, R52LD-5R Technology Derivative	Jan 01

PRODUCT DESCRIPTION (for qualification)		
Qualification Purpose: To qualify: CY62148B, 4Meg SRAM in qualified Derivative R52LD-5R Technology, Fab 4.		
Marketing Part #:	CY62148B	
Device Description::	4.5V-5.5V, Commercial and Industrial available in 32- pins SOIC and 32-lead TSOPII Package	
Cypress Division:	Cypress Semiconductor Corporation – Memory Product Division (MPD)	
Overall Die (or Mask) REV:		Rev. C
What ID markings on Die:	7C62148/7C11483	

TECHNOLOGY/FAB PROCESS DESCRIPTION - R52LD-5R			
Number of Metal Layers:	2	Metal Composition:	Metal 1: 500 Å TiW/6000 Å Al-.5%Cu/300 Å TiW Metal 2: 300Å CoTi /8000Å Al-.5%Cu/300Å TiW
Passivation Type and Materials:	1000Å PECVD Oxide, 9000Å PECVD Si_3N_4		
Free Phosphorus contents in top glass layer(%):	0%		
Number of Transistors in Device:	25million		
Number of Gates in Device:	10 million		
Generic Process Technology/Design Rule (μ-drawn):	CMOS, Double Metal , 0.25 μm/0.3 FETS		
Gate Oxide Material/Thickness (MOS):	70Å (core) 110Å Regulator		
Name/Location of Die Fab (prime) Facility:	Cypress Semiconductor -- Bloomington, MN		
Die Fab Line ID/Wafer Process ID:	Fab4/R52LD-5R		

PACKAGE AVAILABILITY

PACKAGE TYPE	ASSEMBLY SITE FACILITY
44-lead TSSOP II	**OSE Taiwan**
32-lead SOIC	**ASE Taiwan, CSPI-R**

Note: Package Qualification details upon request

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATIPON	
Package Designation:	S32459
Package Outline, Type, or Name:	SOIC
Mold Compound Name/Manufacturer:	NITTO MP8000C
Mold Compound Flammability Rating:	V-O per UL94
Oxygen Rating Index:	＞28%
Lead Frame Material:	Copper
Lead Finish, Composition / Thickness:	Solder Plated 85%Sn, 15%Pb
Die Backside Preparation Method/Metallization:	N/A
Die Separation Method:	Wafer Saw
Die Attach Supplier:	Ablestik
Die Attach Material:	8361H
Bond Diagram Designation	10-03535
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au, 1.0um
Thermal Resistance Theta JA °C/W:	50°C/W
Package Cross Section Yes/No:	N/A
Assembly Process Flow:	49-41003
Name/Location of Assembly (prime) facility:	ASE Taiwan

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	ASE Taiwan
Fault Coverage:	100%

Note: Please contact a Cypress Representative for other packages availability

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	1) QTP #99396 Dynamic Operating Condition, Vcc = 5.75V, 150°C 2) QTP #004405 Dynamic Operating Condition, Vcc = 6.5V, 125°C	P
High Temperature Operating Life Latent Failure Rate	1) QTP #99396 Dynamic Operating Condition, Vcc = 5.75V, 150° 2) QTP #004405 Dynamic Operating Condition, Vcc = 6.5V, 125°C	P
High Accelerated Saturation Test (HAST)	1) QTP #004405 130°C, 85%RH, 5.5V Precondition: JESD22 Moisture Sensitivity MSL 3 (192 hrs, 30C/60%RH+3IR-Reflow, 220°C+5, -0°C)	P
Temperature Cycle	1) QTP 99396, QTP # 004405 MIL-STD-883C, Method 1010, Condition C, -65C to 150C Precondition: JESD22 Moisture Sensitivity MSL3 (192 hrs, 30C/60%RH+3IR-Reflow, 220°C+5, -0°C)	P
Pressure Cooker	1) QTP #99396, QTP #004405 121C, 100%RH Precondition: JESD22 Moisture Sensitivity MSL 3 (192 hrs, 30C/60%RH+3IR-Reflow, 220°C+5, -0°C)	P
Electrostatic Discharge Human Body Model (ESD-HBM)	1) QTP #99396, QTP #004405 MIL-STD-883, Method 3015.7, 2,200V	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	1) QTP 004405, QTP #99396 Cypress Spec. 25-00020 , 500V	P
Current Density	1) QTP #004405 Cypress Spec. 22-00029	P
Acoustic Microscopy/C-SAM	1) QTP #004405 Cypress Spec. 25-00104	P

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT (Continuation)

Stress/Test	Test Condition (Temp/Bias)	Result P/F
Low Temperature Operating Life	1) QTP #004405 -30C, 6.5V, 8MHz	P
Latchup Sensitivity	1) QTP #99396, QTP#004405 125°, 12V, ±300mA In accordance with JEDEC 17. Cypress Spec. 01-00081	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Acceleration Factor[4]	Failure Rate[4]
High Temperature Operating Life Early Failure Rate	4,597	0	N/A	N/A	0 PPM
High Temperature Operating Life[1,2,] Long Term Failure Rate	331,728HRs	0	0.7	170	50 Fit

[1] Assuming an ambient temperature of 150°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate.
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A = The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

[4] **EFR and LFR FIT Rate based on QTP 004405 and 99396.**

Reliability Test Data

QTP #: 004405

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC - MSL3							
CY62148B-SIB	4024870	*610042284*	TAIWN-G	COMP	15	0	
STRESS: ESD-CHARGE DEVICE MODEL (500V)							
CY62148B-SIB	4024870	*610042284*	TAIWN-G	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015 (2,200V)							
CY62148B-SIB	4024870	*610042284*	TAIWN-G	COMP	9	0	
STRESS: HI-ACCEL SATURATION TEST(130C, 85%RH, 5.5V) PRE COND 192 HR 30C/60%RH, MSL3							
CY62148B-SIB	4024870	*610042284*	TAIWN-G	128	48	0	
CY62148B-SCB	4036191	*610045702*	TAIWN-G	240	48	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (125C, 6.5V, Vcc Max)							
CY62148B-ZSC	4024870	*610042301*	KOREA-H	90	1795	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (125C, 6.5V, Vcc Max)							
CY62148B-ZSC	4024870	*610042301*	KOREA-H	500	260	0	
STRESS: LOW TEMPERATURE OPERATING LIFE (-30C, 6.5V, 8MHz)							
CY62148B-SIB	4024870	*610042284*	TAIWN-G	500	24	0	
CY62148B-SIB	4024870	*610042284*	TAIWN-G	500	26	0	
STRESS: PRESSURE COOKER TEST (121C, 100%RH), PRE COND 192 HRS 30C/60%RH, MSL3							
CY62148B-SIB	4024870	*610042284*	TAIWN-G	168	48	0	
STRESS: STATIC LATCH-UP TESTING (125C, 12V, +/-300mA)							
CY62148B-SIB	4024870	*610042284*	TAIWN-G	COMP	3	0	
STRESS: TC CONDITION C,-65C TO 150C, PRE COND. 192 HRS 30C/60%RH (MSL3)							
CY62148B-SIB	4024870	*610042284*	TAIWN-G	300	47	1	OVERBONDING
CY62148B-SIB	4024870	*610042284*	TAIWN-G	1000	45	0	
CY62148B-SCB	4036191	*610045702*	TAIWN-G	300	44	0	
CY62148B-ZCB	4036191	*610045953*	KOREA-H	300	45	0	

Reliability Test Data

QTP #: 99396

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-CDM DONE (500V)							
CY62128B-SC	4020039	*610028034*	CSPI-R	COMP	9	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (150C, 5. 75V, >Vcc Max)							
CY62128B-ZAC	4020039	*610027419*	CSPI-R	48	2802	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (150C, 5. 75V, >Vcc Max)							
CY62128B-ZAC	4020039	*610028034*	CSPI-R	512	394	0	
STRESS: ESD-HBM DONE (2,200V)							
CY62128B-SC	4020039	*610028034*	CSPI-R	COMP	9	0	
STRESS: STATIC LATCH-UP TESTING (125C, 11.5V, +/-300mA)							
CY62128B-SC	4020039	*610028034*	CSPI-R	COMP	3	0	
STRESS: PRESSURE COOKER TEST (121C, 100%RH), PRE COND 192HRS 30C/60%RH							
CY62128B-SC	4020039	*610028034*	CSPI-R	168	50	0	
STRESS: TC CONDITION C, -65C TO 150C, PRE COND. 192 HRS 30C/60% RH (MSL3)							
CY62128B-SC	4020039	*610028034*	CSPI-R	300	50	0	
CY62128B-SC	4020039	*610028034*	CSPI-R	1000	50	0	