

Cypress Semiconductor Product Qualification Report

QTP# 012801 VERSION 1.0
October 2004

4 Meg SRAM Device	
R7LD-1.8 Technology, Fab4	
CY62146CV18 MoBL2™	256K x 16 Static RAM
CY62147CV18 MoBL2™	256K x 16 Static RAM

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

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TECHNOLOGY QUALIFICATION HISTORY

Qual Report	Description of Qualification Purpose	Date Comp
012411	New Technology R7LD-1.8 / New Device, 8Meg, MoBL Static RAM CY62157CV18LL	Jun 01
012801	New Device 4Meg MoBL Static RAM CY62146/7CV18, R7LD-1.8 Technology	Jul 01

PRODUCT DESCRIPTION (for qualification)	
Qualification Purpose: Qualify New Device CY62147CV18 and family R7LD-1.8, Fab 4	
Marketing Part #:	CY62146CV18, CY62147CV18
Device Description:	1.65V – 1.95V, Industrial available in 48-ball FBGA package.
Cypress Division:	Cypress Semiconductor Corporation –Memory Product Division (MPD)
Overall Die (or Mask) REV Level (pre-requisite for qualification):	Rev. C
What ID markings on Die:	7C62345A

TECHNOLOGY/FAB PROCESS DESCRIPTION – R7LD-1.8			
Number of Metal Layers:	2	Metal Composition:	Metal 1: 150Å Ti / 4,200Å Al / 300Å TiW Metal 2: 300Å Ti/8,000 Å Al / 300Å TiW
Passivation Type and Materials:	1000Å TEOS / 9000Å Nitride		
Free Phosphorus contents in top glass layer(%):	0%		
Number of Transistors in Device	50 million		
Number of Gates in Device	3, 512 million		
Generic Process Technology/Design Rule (μ-drawn):	CMOS, Double Metal /0.16 μm		
Gate Oxide Material/Thickness (MOS):	SiO ₂ , 32Å		
Name/Location of Die Fab (prime) Facility:	Cypress Semiconductor -- Bloomington, MN		
Die Fab Line ID/Wafer Process ID:	Fab4/R7-1.8		

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY SITE FACILITY
48-ball FBGA	CML-R, TAIWN-G

Note: Package Qualification details upon request

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	BA48
Package Outline, Type, or Name:	48-ball Fine Pitch Ball Grid Array (FBGA)
Mold Compound Name/Manufacturer:	PLASKON SMT-B-1
Mold Compound Flammability Rating:	V-O per UL94
Oxygen Rating Index:	>28%
Substrate Material:	BT Resin
Lead Finish, Composition / Thickness:	Solder Ball, 63%Sn, 37%Pb
Die Backside Preparation Method/Metallization:	N/A
Die Separation Method:	Wafer Saw
Die Attach Supplier:	Ablestik
Die Attach Material:	Ablestik 8355F
Die Attach Method:	Epoxy
Bond Diagram Designation:	10-04099
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au, 1.0um
Thermal Resistance Theta JA °C/W:	40°C/W
Package Cross Section Yes/No:	N/A
Assembly Process Flow:	49-41020
Name/Location of Assembly (prime) facility:	ASE Taiwan (TAIWN-G)

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	TAIWN-G, CML-R
Fault Coverage:	100%

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc Max = 2.75V, 125°C	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc Max=2.07V, 150°C	P
High Temperature Steady State Life	Static Operating Condition, Vcc Max=1.98V, 150°C	P
High Accelerated Saturation Test (HAST)	130°C, 2.75V, 85%RH Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30C/60%RH+3IR-Reflow, 235°C+5, 0°C	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity MSL3 192 Hrs, 30C/60%RH+3IR-Reflow, 235°C+5, 0°C	P
Pressure Cooker	121°C, 100%RH Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30C/60%RH+3IR-Reflow, 235°C+5, 0°C	P
High Temperature Storage	150°C ± 5°C no bias	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V MIL-STD-883, Method 3015.7	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V Cypress Spec. 25-00020	P
Age Bond Strength	200C, 4HRS MIL-STD-883, Method 883-2011	P
SEM X-Section	MIL-STD-883, Method 883-2018-2 / Cypress Spec. 22-00009	P
Low Temperature Operating Life	-30C, 3.25V, 8MHZ	P
Acoustic Microscopy, MSL 3	Cypress Spec. 25-00104	P
Static Latchup	125C, 6.5V, ± 300mA In accordance with JEDEC 17. Cypress Spec. 01-00081	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF ⁴	Failure Rate
High Temperature Operating Life Early Failure Rate ¹	1540	0	N/A	N/A	0 PPM
High Temperature Operating Life ^{1,2} Long Term Failure Rate	488,288 DHRs	1	0.7	170	24 FIT

¹ A production burn-in of 12 Hrs at 125°C, 2.75V is required for the product.

² Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.

³ Chi-squared 60% estimations used to calculate the failure rate..

⁴ Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp \left[\frac{E_A}{k} \left[\frac{1}{T_2} - \frac{1}{T_1} \right] \right]$$

where:

E_A =The Activation Energy of the defect mechanism.

k = Boltzmann's constant = 8.62x10⁻⁵ eV/Kelvin.

T₁ is the junction temperature of the device under stress and T₂ is the junction temperature of the device at use conditions.

Reliability Test Data

QTP #: 012411

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, 2.75V, Vcc Max							
CY62157CV18LL (7C623571C)	4108785	610112193	CML-R	96	1596	0	
CY62157CV18LL (7C62357C)	4110220	610114276L2	CML-R	96	1246	0	
CY62157CV18LL (7C62357C)	4039754	610100977L1	CML-R	96	791	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 150C, 2.07V, Vcc Max							
CY62157CV18LL (7C623571C)	4107546	610112215	CML-R	96	390	0	
CY62157CV18LL (7C623571C)	4107546	610112215	CML-R	500	389	1	SINGLE BIT FAILURE
CY62157CV18LL (7C623571C)	4108785	610112193	CML-R	96	389	0	
CY62157CV18LL (7C623571C)	4108785	610112193	CML-R	500	388	0	
CY62157CV18LL (7C623571C)	4048795	610103046	CML-R	96	200	0	
CY62157CV18LL (7C623571C)	4048795	610103046	CML-R	500	199	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY62157CV18LL (7C623571C)	4107546	610112305	CML-R	COMP	9	0	
CY62157CV18LL (7C623571C)	4108785	610112193	CML-R	COMP	9	0	
CY62157CV18LL (7C62357C)	4028521	340000332	CML-R	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V							
CY62157CV18LL (7C623571C)	4107546	610112305	CML-R	COMP	9	0	
CY62157CV18LL (7C623571C)	4108785	610112193	CML-R	COMP	9	0	
CY62157CV18LL (7C62357C)	4028521	340000332	CML-R	COMP	9	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 6.5V, +I300mA							
CY62157CV18LL (7C623571C)	4107546	610112305	CML-R	COMP	3	0	
CY62157CV18LL (7C623571C)	4108785	610112193	CML-R	COMP	3	0	
CY62157CV18LL (7C62357C)	4028521	340000332	CML-R	COMP	3	0	
STRESS: ACOUSTIC-MSL3							
CY62157CV18LL (7C623571C)	4107546	610112460	CML-R	COMP	15	0	
CY62157CV18LL (7C623571C)	4107546	610112461	CML-R	COMP	15	0	
CY62157CV18LL (7C623571C)	4107546	610112462	CML-R	COMP	15	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST, 150C, 1.98V, Vcc MAX							
CY62157CV18LL (7C62357C)	4039638	610046995	CML-R	168	77	0	
CY62157CV18LL (7C62357C)	4039638	610046995	CML-R	336	76	1	POLYSILICON PROTRUSION
STRESS: LOW TEMPERATURE OPERATING LIFE, -30C, 3.25V							
CY62157CV18LL (7C62357C)	4039638	610046995	CML-R	500	44	1	POLYSILICON PROTRUSION

Reliability Test Data

QTP #: 012411

<i>Device</i>	<i>Fab Lot #</i>	<i>Assy Lot #</i>	<i>Ass Loc</i>	<i>Duration</i>	<i>Samp</i>	<i>Rej</i>	<i>Failure Mechanism</i>
STRESS: AGE BOND STRENGTH							
CY62157CV18LL (7C623571C)	4107546	610112215	CML-R	COMP	15	0	
CY62157CV18LL (7C62357C)	4111455	610114268	CML-R	COMP	15	0	
CY62157CV18LL (7C62357C)	4110220	610114276L2	CML-R	COMP	15	0	
STRESS: HIGH TEMPERATURE STORAGE, PLASTIC, 150C							
CY62157CV18LL (7C62357C)	4039638	610046995	CML-R	500	48	0	
CY62157CV18LL (7C62357C)	4039638	610046995	CML-R	1000	48	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, PRE COND 192 HR 30C/60%RH, MSL3							
CY62157CV18LL (7C623571C)	4107546	610112305	CML-R	168	54	0	
CY62157CV18LL (7C623571C)	4108785	610112193	CML-R	168	47	0	
CY62157CV18LL (7C62357C)	4111455	610114268L4	CML-R	168	45	0	
STRESS: HI-ACCEL SATURATION TEST, 130C, 85%RH, 1.98V, PRE COND 192 HR 30C/60%RH, MSL3							
CY62157CV18LL (7C62357C)	4039638	610046995	CML-R	128	45	0	
CY62157CV18LL (7C623571C)	4107546	610112215	CML-R	128	50	0	
CY62157CV18LL (7C623571C)	4108785	610112193	CML-R	128	50	0	
STRESS: TC COND. C -65C TO 150C, PRECONDITION 192 HRS 30C/60%RH, MSL3							
CY62157CV18LL (7C62357C)	4039638	610046995	CML-R	300	46	0	
CY62157CV18LL (7C623571C)	4107546	610112215	CML-R	300	102	0	
CY62157CV18LL (7C623571C)	4108785	610112193	CML-R	300	47	0	

Reliability Test Data

QTP #: 012801

<i>Device</i>	<i>Fab Lot #</i>	<i>Assy Lot #</i>	<i>Ass Loc</i>	<i>Duration</i>	<i>Samp</i>	<i>Rej</i>	<i>Failure Mechanism</i>
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, 2.75V, Vcc Max							
CY62147CV18LL (7C62347C)	4115508	610120017	CML-R	96	1540	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY62147CV18LL (7C62347C)	4045021	610101961	CML-R	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V							
CY62147CV18LL (7C62347C)	4045021	610101961	CML-R	COMP	9	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 6.5V, +I300mA							
CY62147CV18LL (7C62347C)	4045021	610101961	CML-R	COMP	9	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, PRE COND 192 HR 30C/60%RH, MSL3							
CY62147CV18LL (7C62347C)	4045021	610101961	CML-R	168	50	0	
CY62147CV18LL (7C62347C)	4113906	610117246	CML-R	168	49	0	
STRESS: TC COND. B -5C TO 125C, PRECONDITION 192 HRS 30C/60%RH, MSL3							
CY62147CV18LL (7C62347C)	4045021	610101961	CML-R	500	50	0	
CY62147CV18LL (7C62347C)	4045021	610101961	CML-R	1500	50	0	
CY62147CV18LL (7C62347C)	4045021	610101961	CML-R	2000	47	0	