Cypress Semiconductor
Technology Qualification Report

QTP# 012407 VERSION 1.2
November 2002

Synchronous SRAM Family R63D-25 Technology, Fab4	
CY7C1354V25	**256K x 36 200MHz**
CY7C1356V25	**512K x 18 200MHz**

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PRODUCT QUALIFICATION HISTORY

Qual Report	Description of Qualification Purpose	Date Comp
011308	New Technology R63D-25 / New Product, 8Meg, Pipelined SRAM with NoBL™ Architecture CY7C1354V25. **Production Qualification, not full Qualification**	Apr 01
012407	New Technology R63D-25 / New Product, 8Meg, Pipelined SRAM with NoBL™ Architecture CY7C1354V25. **Full Qualification**	Jun 01

PRODUCT DESCRIPTION (for qualification)			
Qualification Purpose: Qualify New Technology R63D-25, Fab 4 and CY7C1354V25, product family and metal option.			
Marketing Part #:	CY7C1354V25/CY7C1356V25		
Device Description:	2.5V, Commercial available in 100-pin TQFP and 119-Ball BGA package.		
Cypress Division:	Cypress Semiconductor Corporation – Synchronous Memory Product Division (SMPD)		
Overall Die (or Mask) REV Level (pre-requisite for qualification):		Rev. A	
What ID markings on Die:	7C1354A		

TECHNOLOGY/FAB PROCESS DESCRIPTION - R63D-25			
Number of Metal Layers:	2	Metal Composition:	Metal 1: 500Å TiW/6,000Å AlCu/300Å TiW Metal 2: 500Å TiW/8,000Å AlCu/300Å TiW
Passivation Type and Materials:	1000Å PECVD oxide / 9000Å PECVD		
Free Phosphorus contents in top glass layer (%):	0%		
Number of Transistors in Device	60 million		
Number of Gates in Device	20 million		
Generic Process Technology/Design Rule (μ-drawn):	CMOS, Double Metal /0.27 μm		
Gate Oxide Material/Thickness (MOS):	SiO_2, 55 Å		
Name/Location of Die Fab (prime) Facility:	Cypress Semiconductor -- Bloomington, MN		
Die Fab Line ID/Wafer Process ID:	Fab4/R63D-25		

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY SITE FACILITY
119-Ball BGA	**ASE, TAIWN-G**
100-Pin TQFP	**CSPI-R**

Note: Package Qualification details upon request

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	A100
Package Outline, Type, or Name:	100-Thin Quad Flat Pack (TQFP)
Mold Compound Name/Manufacturer:	Hitachi CEL 9200
Mold Compound Flammability Rating:	V-O per UL94
Oxygen Rating Index:	>28%
Lead Frame Material:	Copper
Lead Finish, Composition / Thickness:	Solder Plate, 90%Sn, 10%Pb
Die Backside Preparation Method/Metallization:	N/A
Die Separation Method:	Wafer Saw
Die Attach Supplier:	Ablestik
Die Attach Material:	Ablestik 8355
Die Attach Method:	Epoxy
Bond Diagram Designation:	10-03700
Wire Bond Method:	Thermo sonic
Wire Material/Size:	Au, 1.0um
Thermal Resistance Theta JA °C/W:	50°C/W
Package Cross Section Yes/No:	N/A
Assembly Process Flow:	11-20005
Name/Location of Assembly (prime) facility:	Cypress Philippines (CSPI-R)

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	Cypress Philippines (CSPI-R)
Fault Coverage:	100%

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc Max = 2.88V, 150°C	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc Max=2.88V, 150°C	P
High Temperature Steady State Life	Static Operating Condition, Vcc Max=2.75V, 150°C	P
High Accelerated Saturation Test (HAST)	130°C, 2.75V, 85%RH Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30C/60%RH+3IR-Reflow, 235°C+0, -5°C	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30C/60%RH+3IR-Reflow, 235°C+05, -5°C	P
Pressure Cooker	121°C, 100%RH Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30C/60%RH+3IR-Reflow, 235°C+0, -5°C	P
High Temperature Storage	150°C ± 5°C no bias	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V MIL-STD-883, Method 3015.7	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V Cypress Spec. 25-00020	P
Age Bond Strength	200C, 4HRS MIL-STD-883, Method 883-2011	P
SEM X-Section	MIL-STD-883, Method 883-2018-2 / Cypress Spec. 22-00009	P
Low Temperature Operating Life	-30C, 3.25V, 8MHZ	P
Acoustic Microscopy, MSL 3	Cypress Spec. 25-00104	P
Current Density	Cypress Spec 22-00029	P
Dynamic Latch up	4.3V In accordance with JEDEC 17. Cypress Spec. 01-00081	P
Static Latch up	125C, 8V, ± 300mA In accordance with JEDEC 17. Cypress Spec. 01-00081	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[4]	Failure Rate
High Temperature Operating Life Early Failure Rate[1]	1,610 Devices	0	N/A	N/A	0 PPM
High Temperature Operating Life[1,2] Long Term Failure Rate	765,940 DHRS	3	0.7	170	23 FIT

[1] A production burn-in of 12 Hrs at 150°C, 3.1V is required for the product.
[2] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[3] Chi-squared 60% estimations used to calculate the failure rate..
[4] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

Reliability Test Data

QTP #: 011308

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-CHARGE DEVICE MODEL (500V)							
CY7C1354V25-AC (7C13542A)	4026207	*610040521*	CSPI-R	COMP	9	0	
CY7C1354V25-AC (7C13542A)	4030860	*610042556*	CSPI-R	COMP	9	0	
CY7C1354V25-AC (7C13542A)	4031097	*610044277/960*	CSPI-R	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015 (2,200V)							
CY7C1354V25-AC (7C13542A)	4026207	*610040521*	CSPI-R	COMP	9	0	
CY7C1354V25-AC (7C13542A)	4030860	*610042556*	CSPI-R	COMP	9	0	
CY7C1354V25-AC (7C13542A)	4031097	*610044277/960*	CSPI-R	COMP	9	0	
STRESS: STATIC LATCH-UP TESTING (125C, 8V, +/300mA)							
CY7C1354V25-AC (7C13542A)	4026207	*610040521*	CSPI-R	COMP	3	0	
CY7C1354V25-AC (7C13542A)	4030860	*610042556*	CSPI-R	COMP	3	0	
CY7C1354V25-AC (7C13542A)	4031097	*610044277/960*	CSPI-R	COMP	3	0	
STRESS: DYNAMIC LATCH-UP TESTING (4.3V)							
CY7C1354V25-AC (7C13542A)	4023631	*610040522N*	CSPI-R	COMP	3	0	
STRESS: ACOUSTIC-MSL3							
CY7C1354V25-AC (7C13542A)	4026207	*610040521*	CSPI-R	COMP	15	0	
CY7C1354V25-AC (7C13542A)	4030860	*610042556*	CSPI-R	COMP	15	0	
CY7C1354V25-AC (7C13542A)	4031097	*610044277/960*	CSPI-R	COMP	15	0	
STRESS: AGE BOND STRENGTH							
CY7C1354V25-AC (7C13542A)	4026207	*610040521*	CSPI-R	COMP	10	0	
CY7C1354V25-AC (7C13542A)	4030860	*610042556*	CSPI-R	COMP	15	0	
CY7C1354V25-AC (7C13542A)	4031097	*610044277/960*	CSPI-R	COMP	15	0	
STRESS: HIGH TEMPERATURE STORAGE, PLASTIC, 150C							
CY7C1354V25-AC (7C13542A)	4016340	*610023602*	CSPI-R	500	50	0	
CY7C1354V25-AC (7C13542A)	4016340	*610023602*	CSPI-R	1000	50	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST (150C, 2.75V, Vcc MAX)							
CY7C1354V25-AC (7C13542A)	4026207	*610040521*	CSPI-R	80	78	0	
CY7C1354V25-AC (7C13542A)	4026207	*610040521*	CSPI-R	168	78	0	
STRESS: AGE BOND STRENGTH							
CY7C1354V25-AC (7C13542A)	4026207	*610040521*	CSPI-R	COMP	10	0	
CY7C1354V25-AC (7C13542A)	4030860	*610042556*	CSPI-R	COMP	15	0	
CY7C1354V25-AC (7C13542A)	4031097	*610044277/960*	CSPI-R	COMP	15	0	

Reliability Test Data

QTP #: 011308

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: PRESSURE COOKER TEST (121C, 100%RH), PRE CONDITION 192 HR 30C/60%RH (MSL3)							
CY7C1354V25-AC (7C13542A)	4026207	*610040521*	CSPI-R	168	47	0	
CY7C1354V25-AC (7C13542A)	4030860	*610042556*	CSPI-R	168	48	0	
CY7C1354V25-AC (7C13542A)	4031097	*610044277/960*	CSPI-R	168	48	0	
STRESS: HI-ACCEL SATURATION TEST (130C, 85%RH, 2.75V), PRE CONDITION 192 HR 30C/60%RH (MSL3)							
CY7C1354V25-AC (7C13542A)	4026207	*610040521*	CSPI-R	128	48	0	
CY7C1354V25-AC (7C13542A)	4030860	*610042556*	CSPI-R	128	48	0	
CY7C1354V25-AC (7C13542A)	4030860	*610042556*	CSPI-R	256	48	0	
CY7C1354V25-AC (7C13542A)	4031097	*610044277/960*	CSPI-R	128	48	0	
STRESS: TC COND. C -65C TO 150C, PRE CONDITION 192 HRS 30C/60%RH (MSL3)							
CY7C1354V25-AC (7C13542A)	4026207	*610040521*	CSPI-R	421	46	0	
CY7C1354V25-AC (7C13542A)	4016340	*610023602*	CSPI-R	300	48	0	
CY7C1354V25-AC (7C13542A)	4016340	*610023602*	CSPI-R	500	48	0	
CY7C1354V25-AC (7C13542A)	4031097	*610044277/960*	CSPI-R	300	48	0	
CY7C1354V25-AC (7C13542A)	4031097	*610044277/960*	CSPI-R	500	48	0	
CY7C1354V25-AC (7C13542A)	4031097	*610044277/960*	CSPI-R	1000	48	0	
STRESS: LOW TEMPERATURE OPERATING LIFE (-30C, 3.25V)							
CY7C1354V25-AC (7C13542A)	4031097	*610044277/960*	CSPI-R	500	48	0	

Reliability Test Data

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Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (150C, 2.88V, Vcc Max)							
CY7C1354V25-AC (7C13542A)	4040911	*610052716*	CSPI-R	48	530	0	
CY7C1354V25-AC (7C13542A)	4045033	*610107635*	CSPI-R	48	530	0	
CY7C1354V25-AC (7C13542A)	4051654	*610113654*	CSPI-R	48	550	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (150C, 2.88V, Vcc Max)							
CY7C1354V25-AC (7C13542A)	4040911	*610052716*	CSPI-R	80	530	0	
CY7C1354V25-AC (7C13542A)	4040911	*610052716*	CSPI-R	500	523	3	SB=POLY DEFECT NON VISUAL IN 2 UNITS
CY7C1354V25-AC (7C13542A)	4045033	*610107635*	CSPI-R	80	530	0	
CY7C1354V25-AC (7C13542A)	4045033	*610107635*	CSPI-R	500	527	0	
CY7C1354V25-AC (7C13542A)	4051654	*610113654*	CSPI-R	80	550	0	
CY7C1354V25-AC (7C13542A)	4051654	*610113654*	CSPI-R	500	464	0	