Cypress Semiconductor
Product Qualification Report

QTP# 011503 VERSION 1.0
December 2005

Spread Spectrum Timing Solution for Serverworks Chipset L28 Technology, Fab 2	
CY28158	**100-133 MHz**

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

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PRODUCT QUALIFICATION HISTORY

Qual Report		Description of Qualification Purpose		Date Comp
97403		New Technology L28/New Device CY227*		Apr 98
011503		New Device CY28158PVC, L28 Technology		Apr 01

PRODUCT DESCRIPTION (for qualification)	
Qualification Purpose: Qualify CY28158 in L28 Technology, Fab 2.	
Marketing Part #:	CY28158
Device Description:	3.3V, Commercial available in 56-Lead SSOP Package.
Cypress Division:	Cypress Semiconductor Corporation – Consumer & Computation Division (CCD)
Overall Die (or Mask) REV Level (pre-requisite for qualification):	Rev. A
What ID markings on Die:	7C81500A

TECHNOLOGY/FAB PROCESS DESCRIPTION - L28			
Number of Metal Layers:	2	Metal Composition:	Metal 1: 500A Ti/1,200A TiW/6,000A Al/1,200A TiW Metal 2: 1,500A TiW//10,000A Al/150A Ti
Passivation Type and Materials:	3,000A TEOS + 15,000A Si_2N_4		
Free Phosphorus contents in top glass layer (%):	N/A		
Die Coating(s), if used:	N/A		
Generic Process Technology/Design Rule (μ-drawn):	CMOS, Single Poly, Double Metal /0.65 μm		
Gate Oxide Material/Thickness (MOS):	SiO_2 / 145 A		
Name/Location of Die Fab (prime) Facility:	Cypress Semiconductor - Round Rock, TX		
Die Fab Line ID/Wafer Process ID:	Fab2/L28		

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY FACILITY SITE
56-Lead SSOP	**CML-R**

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	056
Package Outline, Type, or Name:	56-lead Shrunk Small Outline Package (SSOP)
Mold Compound Name/Manufacturer:	Hitachi CEL 9200
Mold Compound Flammability Rating:	V-O per UL94
Oxygen Rating Index:	>28%
Lead Frame Material:	Copper
Lead Finish, Composition / Thickness:	Solder Plated, 85%Sn, 15%Pb
Die Backside Preparation Method/Metallization:	N/A
Die Separation Method:	Wafer Saw
Die Attach Supplier:	Ablestik
Die Attach Material:	8361H
Bond Diagram Designation	10-04172
Wire Bond Method:	Thermosonic
Wire Material/Size:	1.0 mil
Thermal Resistance Theta JA °C/W:	54.9°C/W
Package Cross Section Yes/No:	N/A
Assembly Process Flow:	11-20048
Name/Location of Assembly (prime) facility:	Cypress Philippines (CML-R)

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	CML-R
Fault Coverage:	100%

Note: Please contact a Cypress Representative for other packages availability.

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc = 3.65V, 150C	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc = 3.65V, 150C	P
Read and Record	Dynamic Operating Condition, Vcc = 3.65V, 150C	P
High Accelerated Saturation Test (HAST)	140°C, 85%RH, 3.63V Precondition: JESD22 Moisture Sensitivity Level 1 168 Hrs, 85°C/85%RH +3IR-Reflow, 220°C+0, -5°C	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity Level 1 168 Hrs, 85°C/85%RH+3IR-Reflow, 220°C+0, -5°C	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V/4,000V MIL-STD-883, Method 3015.7	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V/1,000V Cypress Spec. 25-00020	P
High Temperature Storage	165C, no bias	P
Data Retention	165C, no bias	P
Cold Life Test	-30C, 6.5V	P
Latch up Sensitivity	125C, +/-300mA In accordance with JEDEC 17. Cypress Spec. 01-00081	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal[3] A.F	Failure Rate
High Temperature Operating Life Early Failure Rate	850 Devices	0	N/A	N/A	0 PPM
High Temperature Operating Life[1,2] Long Term Failure Rate	173,900 DHRs	0	0 .7	170	31 FITs

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate.
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

Reliability Test Data

QTP #: 97403

Device	Assy Loc.	Fab Lot#	Assy Lot#	Duration	S/S	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (150C, 3.65V)							
CY2273APVC	CSPI-R	2732995	619708289/319	48	180	0	
CY2273APVC	CSPI-R	2735423	619709731	48	340	0	
CY2273APVC	CSPI-R	2734307	619709732	48	330	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (150C, 3.65V)							
CY2273APVC	CSPI-R	2732995	619708289/319	80	116	0	
CY2273APVC	CSPI-R	2732995	619708289/319	500	116	0	
CY2273APVC	CSPI-R	2735423	619709731	80	120	0	
CY2273APVC	CSPI-R	2735423	619709731	500	116	0	
CY2273APVC	CSPI-R	2734307	619709732	80	116	0	
CY2273APVC	CSPI-R	2734307	619709732	500	115	0	
STRESS: READ & RECORD LIFE TEST (150C, 3.65V)							
CY2273APVC	CSPI-R	2734307	619709732	48	10	0	
CY2273APVC	CSPI-R	2734307	619709732	80	10	0	
CY2273APVC	CSPI-R	2734307	619709732	500	10	0	
STRESS: COLD LIFE TEST (-30C, 6.5V)							
CY2273APVC	CSPI-R	2732995	619708289/319	500	45	0	
CY2273APVC	CSPI-R	2732995	619708289/319	1000	44	0	
STRESS: ESD-CHARGE DEVICE MODEL, 1,000V							
CY2273APVC	CSPI-R	2732995	619708289/319	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 4,000V							
CY2273APVC	CSPI-R	2732995	619708289/319	COMP	3	0	
STRESS: DATA BAKE-PLASTIC (165C, NO BIAS)							
CY2273APVC	CSPI-R	2732995	619708289/319	168	78	0	
CY2273APVC	CSPI-R	2732995	619708289/319	552	78	0	
CY2273APVC	CSPI-R	2735423	619709731	168	78	0	
CY2273APVC	CSPI-R	2735423	619709731	552	78	0	
CY2273APVC	CSPI-R	2734307	619709732	168	78	0	
CY2273APVC	CSPI-R	2734307	619709732	552	78	0	

Reliability Test Data

QTP #: 97403

Device	Assy Loc.	Fab Lot#	Assy Lot#	Duration	S/S	Rej	Failure Mechanism
STRESS: HIGH TEMPERATURE STORAGE (165C, NO BIAS)							
CY2273APVC	CSPI-R	2732995	619708289/319	336	45	0	
CY2273APVC	CSPI-R	2732995	619708289/319	500	45	0	
CY2273APVC	CSPI-R	2732995	619708289/319	1000	45	0	
STRESS: HI-ACCEL SATURATION TEST (140C, 3.63V), PRE COND, 168 HRS 85C/85%RH, MSL1							
CY2273APVC	CSPI-R	2732995	619708289/319	128	44	0	
CY2273APVC	CSPI-R	2732995	619708289/319	256	44	0	
CY2273APVC	CSPI-R	2734307	619709732	128	45	0	
STRESS: TC COND. C, -65 TO 150C, PRE COND, 168 HRS 85C/85%RH, MSL1							
CY2273APVC	CSPI-R	2732995	619708289/319	300	45	0	
CY2273APVC	CSPI-R	2732995	619708289/319	1000	45	0	
CY2273APVC	CSPI-R	2735423	619709731	300	48	0	
CY2273APVC	CSPI-R	2735423	619709731	1000	48	0	
CY2273APVC	CSPI-R	2734307	619709732	300	47	0	
CY2273APVC	CSPI-R	2734307	619709732	1000	47	0	

Reliability Test Data

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Device	*Fab Lot #*	*Assy Lot #*	*Assy Loc*	*Duration*	*Samp*	*Rej*	*Failure Mechanism*
STRESS: ESD-CHARGE DEVICE MODEL (500V)							
CY28158PVC-OC (7C81500A)	210508	*610112963*	CSPI-R	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015 (2,200V)							
CY28158PVC-OC (7C81500A)	210508	*610112963*	CSPI-R	COMP	9	0	
STRESS: STATIC LATCH-UP TESTING (125C, 12V, +/-300mA)							
CY28158PVC-OC (7C81500A)	210508	*610112963*	CSPI-R	COMP	3	0	