

# Cypress Semiconductor Technology Qualification Report

011103 VERSION 1.2

April, 2001

<b>WaferTech 0.25um 3P2M Process Technology WA USA</b>					
Option #	CYP	Description			
		GVT Product	Vcc	Arch.	Config.
1	7C1347D	GVT71128D36V (TMB057A01A)	3.3V	PL-1CD	128k x 36
2	7C1348D	GVT71128C36V (TMB057A01A)	3.3V	PL-2CD	128k x 36
3	7C1327D	GVT71256D18V (TMB057A02A)	3.3V	PL-1CD	256k x 18
4	7C1328D	GVT71256C18V (TMB057A02A)	3.3V	PL-2CD	256k x 18
5	7C1359A	GVT71256T18V (TMB057A02A)	3.3V	PL-1CD (TAG)	256k x 18
6	7C1345D	GVT71128B36V (TMB057xxxx)	3.3V	FT	128k x 36
7	7C1347D	GVT71128G36V (TMB057A01A)	3.3V	PL-1CD	128k x 36
8	na	GVT71128F36V (TMB057A01A)	3.3V	PL-2CD	128k x 36
9	7C1325D	GVT71256B18V (TMB057xxxx)	3.3V	FT	128k x 36
10	7C1345D	GVT71128E36V (TMB057xxxx)	3.3V	FT	128k x 36
11	7C1347C	GVT71128DA36V (TMB057C01A)	3.3V	PL-1CD	128k x 36
12	na	GVT71128CA36V (TMB057C01A)	3.3V	PL-2CD	128k x 36
13	7C1327C	GVT71256DA18V (TMB057C02A)	3.3V	PL-1CD	256k x 18
14	na	GVT71256CA18V (TMB057C02A)	3.3V	PL-2CD	256k x 18

## CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

Ed Russell  
Reliability Director  
(408) 432-7069

Kim-Ngan Nguyen  
Staff Reliability Engineer  
(408) 943-2136

### PRODUCT QUALIFICATION HISTORY

<b>Qual Report</b>	<b>Description of Qualification Purpose</b>	<b>Date Comp</b>
011103	WaferTech .25um Technology / 4Meg, GVT71128D36 (CY7C1347D) product and its bond and metal options	Mar 01

<b>PRODUCT DESCRIPTION (for qualification)</b>	
Qualification Purpose: Qualify WaferTech .25um Technology and 4Meg, GVT71128D36 (CY7C1347D) product and its bond and metal options.	
Marketing Part #:	GVT71128D36* (CY7C1347D)
Device description:	3.3V, Commercial available in 100-pin TQFP and 119-ball BGA package
Cypress Division:	Cypress Semiconductor Corporation – Synchronous Memory Product Division (SMPD)
Overall Die (or Mask) REV Level (pre-requisite for qualification):	Rev. D
What ID markings on Die:	GVT71128DA36W

<b>TECHNOLOGY/FAB PROCESS DESCRIPTION</b>			
Number of Metal Layers:	2	Metal Composition:	Metal 1: 4,000Å AlCu/.700Å TiN Metal 2: 1,000Å TiN/6,000Å AlCu/250Å TiN
Passivation Type and Materials:	1,500Å SiON / 5,000Å SOG/10,000Å PESN		
Free Phosphorus contents in top glass layer(%):	0		
Generic Process Technology/Design Rule (μ-drawn):	CMOS, Double Metal / 0.25um		
Gate Oxide Material/Thickness (MOS):	SiO <sub>2</sub> / 70Å		
Name/Location of Die Fab (prime) Facility:	WaferTech, WA USA		
Die Fab Line ID/Wafer Process ID:	WaferTech 0.25um 3P2M Process Technology		

#### PACKAGE AVAILABILITY

<b>PACKAGE</b>	<b>ASSEMBLY SITE FACILITY</b>
100-pin TQFP	ASE/SPIL
119-ball BGA (qualified by extension of 292-ball)	ASE

**Note:** Package Qualification details upon request

<b>MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION</b>	
<b>Package Designation:</b>	A100
<b>Package Outline, Type, or Name:</b>	100-pin, Thin Quad Flat Pack (TQFP)
<b>Mold Compound Name/Manufacturer:</b>	Hitachi 7320
<b>Mold Compound Flammability Rating:</b>	V-O per UL94
<b>Oxygen Rating Index:</b>	> 28 %
<b>Lead Frame Material:</b>	Copper
<b>Lead Finish, Composition / Thickness:</b>	Solder Plate, 85 % Sn, 15 % Pb
<b>Die Backside Preparation Method/Metallization:</b>	N/A
<b>Die Separation Method:</b>	Wafer Saw
<b>Die Attach Supplier:</b>	Sumitomo
<b>Die Attach Material:</b>	Sumitomo 1076A
<b>Bond Diagram Designation</b>	10-04091
<b>Wire Bond Method:</b>	Thermosonic
<b>Wire Material/Size:</b>	Au, 1.0um
<b>Thermal Resistance Theta JA °C/W:</b>	51°C/W
<b>Package Cross Section Yes/No:</b>	N/A
<b>Assembly Process Flow:</b>	GVT164-04-000-0053/FC-2800
<b>Name/Location of Assembly (prime) facility:</b>	ASE/SPIL

<b>ELECTRICAL TEST / FINISH DESCRIPTION</b>	
<b>Test Location:</b>	ASE/CHIPMOS
<b>Fault Coverage:</b>	100 %

**RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT**

<b>Stress/Test</b>	<b>Test Condition (Temp/Bias)</b>	<b>Result P/F</b>
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc Max=3.8V, 150°C	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc Max=3.8V, 150°C	P
High Accelerated Saturation Test (HAST)	130°C, 5.5V, 85%RH Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30C/60%RH+3IR-Reflow, 220°C+5, 0°C	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30C/60%RH+3IR-Reflow, 220°C+5, 0°C	P
Pressure Cooker	121°C, 100%RH Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30C/60%RH+3IR-Reflow, 220°C+5, 0°C	P
High Temperature Steady State life	150°C, 3.63V, Vcc Max	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V MIL-STD-883, Method 3015.7	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	200V Cypress Spec. 25-00020	P
Age Bond Strength	MIL-STD-883, Method 883-2011, 200C, 4hrs	P
SEM -X Section	MIL-STD-883, Method 883-2018-2	P
Acoustic Microscopy, MSL3	Cypress Spec. 25-00104	P
Low Temperature Operating Life	-30C, 3.3V, 8MHZ	P
Latchup Sensitivity	125°, ± 300mA In accordance with JEDEC 17. Cypress Spec. 01-00081	P

**RELIABILITY FAILURE RATE SUMMARY**

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF <sup>3</sup>	Failure Rate
High Temperature Operating Life Early Failure Rate <sup>1</sup>	2,991	1	N/A	N/A	334 PPM
High Temperature Operating Life <sup>2,3</sup> Long Term Failure Rate	794,580 DHRs	1	0.7	150	14.9 FIT

<sup>1</sup> A production burn-in of 5 Hrs at 125°C, 4.2V is required for the product

<sup>2</sup> Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.

<sup>3</sup> Chi-squared 60% estimations used to calculate the failure rate.

<sup>4</sup> Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp \left[ \frac{E_A}{k} \left[ \frac{1}{T_2} - \frac{1}{T_1} \right] \right]$$

where:

E<sub>A</sub> =The Activation Energy of the defect mechanism.

k = Boltzmann's constant = 8.62x10<sup>-5</sup> eV/Kelvin.

T<sub>1</sub> is the junction temperature of the device under stress and T<sub>2</sub> is the junction temperature of the device at use conditions.

## Reliability Test Data

QTP #: 011103

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
<b>STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (150C, 3.8V, Vcc Max)</b>							
GVT71128G36* (7C1347D)	W60325	W60325DA	SPIL	48	982	1	BAKE RECOVERED, NON VISUAL
GVT71256T18* (7C1359A)	W26921	W26921AB	SPIL	48	1008	0	
GVT71256T18* (7C1359A)	W26998	W26998AB	SPIL	48	1000	0	
<b>STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (150C, 3.8V, Vcc Max)</b>							
GVT71128G36* (7C1347D)	W60325	W60325DA	SPIL	80	530	0	
GVT71128G36* (7C1347D)	W60325	W60325DA	SPIL	500	530	0	
GVT71256T18* (7C1359A)	W26921	W26921AB	SPIL	80	529	1	SINGLE BIT FAILURE
GVT71256T18* (7C1359A)	W26921	W26921AB	SPIL	500	529	0	
GVT71256T18* (7C1359A)	W26998	W26998AB	SPIL	80	530	0	
GVT71256T18* (7C1359A)	W26998	W26998AB	SPIL	500	530	0	
<b>STRESS: HI-ACCEL SATURATION TEST (130C, 85%RH, 3.63V)PRE COND 192 HR 30C/60%RH</b>							
GVT71256D36*(7C1360A)	W90760	W90760.02	SPIL	128	48	0	
<b>STRESS: PRESSURE COOKER TEST (121C, 100%RH), PRE COND 192HRS 30C/60%RH</b>							
GVT71256D36*(7C1360A)	W90760	W90760.02	SPIL	168	47	0	
<b>STRESS: ESD-CHARGE DEVICE MODEL (200V)</b>							
GVT71128DA36* (7C1347C)	W30857	W30857AB	SPIL	COMP	9	0	
<b>STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015 (2,200V)</b>							
GVT71128DA36* (7C1347C)	W30857	W30857AB	SPIL	COMP	9	0	
<b>STRESS: STATIC LATCH-UP TESTING (125C, +/300mA)</b>							
GVT71256T18* (7C1359A)	W26998	W26998AB	SPIL	COMP	3	0	
<b>STRESS: ACOUSTIC-MSL3</b>							
GVT71128G36* (7C1347D)	W60325	W60325DA	SPIL	COMP	15	0	
<b>STRESS: AGE BOND STRENGTH TEST</b>							
GVT71256D36*(7C1360A)	W90760	W90760.02	SPIL	COMP	15	0	
GVT71256D36*(7C1360A)	W18916	W18916.02	SPIL	COMP	15	0	
<b>STRESS: HIGH TEMP STEADY STATE LIFE TEST (150C, 3.63V, Vcc MAX)</b>							
GVT71128G36* (7C1347D)	W60325	W60325DA	SPIL	80	80	0	
GVT71128G36* (7C1347D)	W60325	W60325DA	SPIL	168	80	0	

## Reliability Test Data

QTP #: 011103

<i>Device</i>	<i>Fab Lot #</i>	<i>Assy Lot #</i>	<i>Assy Loc</i>	<i>Duration</i>	<i>Samp</i>	<i>Rej</i>	<i>Failure Mechanism</i>
<b>STRESS: TC CONDITION C, -65C TO 150C, PRE COND. 192 HRS 30C/60% RH (MSL3)</b>							
GVT71256D36*(7C1360A)	W90760	W90760.02	SPIL	300	50	0	
GVT71256D36*(7C1360A)	W90760	W90760.02	SPIL	500	50	0	
GVT71256D36*(7C1360A)	W18916	W18916.02	SPIL	300	49	0	
GVT71256D36*(7C1360A)	W18916	W18916.02	SPIL	500	49	0	
GVT71256D36*(7C1360A)	W18946	W18946.02	SPIL	1000	48	0	
GVT71256D36*(7C1360A)	W18746	W18746.02	SPIL	300	48	0	
GVT71256D36*(7C1360A)	W18746	W18746.02	SPIL	500	47	0	
GVT71256D36*(7C1360A)	W18746	W18746.02	SPIL	1000	47	0	
<b>STRESS: LOW TEMPERATURE OPERATING LIFE (-30C, 3.3V)</b>							
GVT71256D36*(7C1360A)	W18916	W18916.02	SPIL	500	48	0	