Cypress Semiconductor
Product Qualification Report

QTP #002704 VERSION 1.1
May, 2001

3Meg Fast Asynchronous SRAM WaferTech .35um Technology	
CY7C1024AV33	**128K x 24 Static RAM**

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

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Product Qualification History

Qual Report	Description of Qualification Purpose	Date Comp
GVT	New WaferTech .35um Technology 4T Process / GVT171128E36, 4Meg	Jan 98
GVT	New Product GVT73128A24, WaferTech .35um Technology	Nov 99
002704	New CY7C1024AV33, 3Meg Synchronous SRAM / WaferTech .35um Technology 4T Process	Mar 01

Cypress products are manufactured using qualified processes. The technology qualification for this product is referenced above and must be considered to get a complete and thorough evaluation of the reliability of the product.

PRODUCT DESCRIPTION (for qualification)		
Qualification Purpose: Qualify CY7C1024AV33 in qualified WaferTech .35um Technology 4T Process.		
Marketing Part #:	CY7C1024AV33	
Device description:	3.3V, Commercial; and Industrial available in 119-bal BGA and 100-pin TQFP package	
Cypress Division:	Cypress Semiconductor Corporation – Synchronous Memory Product Division (MPD)	
Overall Die (or Mask) REV Level (pre-requisite for qualification):		Rev. V
What ID markings on Die:	GVT73128A24Z	

TECHNOLOGY/FAB PROCESS DESCRIPTION			
Number of Metal Layers:	2	Metal Composition:	Metal 1: 4KÅ Ti/1KÅ TiN/4KÅ AlCu/.25KÅ TiN Metal 2: 1,5KÅ ATi/6KÅ AlCu/.25KÅ TiN
Passivation Type and Materials:	2K PE-Oxide + 6.5K PE-Nitride		
Free Phosphorus contents in top glass layer(%):	0		
Generic Process Technology/Design Rule (μ-drawn):	0.35um		
Gate Oxide Material/Thickness (MOS):	70A SiO2		
Name/Location of Die Fab (prime) Facility:	WaferTech, WA USA		
Die Fab Line ID/Wafer Process ID:	WaferTech 0.35um 4T SRAM TPDM Process Flow		

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY SITE FACILITY
100-pin TQFP	**ASE / ASEK**
119-ball BGA	**ASE**

Note: Package Qualification details upon request

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	BG119
Package Outline, Type, or Name:	119-ball, Ball Grid Array (BGA)
Mold Compound Name/Manufacturer:	Plaskon SMT B I
Mold Compound Flammability Rating:	V-O per UL94
Oxygen Rating Index:	>28%
Substrate Material:	BT Resin
Lead Finish, Composition / Thickness:	Solder Ball, 63%Sn, 37%Pb
Die Backside Preparation Method/Metallization:	N/A
Die Separation Method:	Wafer Saw
Die Attach Supplier:	Ablestik
Die Attach Material:	Ablestik 8355
Bond Diagram Designation	10-03823
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au, 1.0um
Thermal Resistance Theta JA °C/W:	57°C/W
Package Cross Section Yes/No:	N/A
Assembly Process Flow:	49-41008
Name/Location of Assembly (prime) facility:	ASE Taiwan (TAIWN-G)

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	ASE Taiwan (TAIWN-G)
Fault Coverage:	100%

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc = 3.8V, 125°C	P
High Accelerated Saturation Test (HAST)	1) QTP #002704 130°C, 3.63V,85%RH Precondition: JESD22 Moisture Sensitivity Level 3 (192 Hrs, 30C/60%RH+3IR-Reflow, 220°C+5, 0°C)	P
Temperature Cycle	1) QTP #002704 MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity Level 3 (192 Hrs, 30C/60%RH+3IR-Reflow, 220°C+5, 0°C)	P
Pressure Cooker	1) QTP #002704 Precondition: JESD22 Moisture Sensitivity Level 3 (192 Hrs, 30C/60%RH+3IR-Reflow, 220°C+5, 0°C)	P
Human Body Model (ESD-HBM)	MIL-STD-883, Method 3015.7 (2,000V)	P
Charge Device Model (ESD-CDM)	1) QTP #002704 Cypress Spec. 25-00020 (500V)	P
Thermal Shock	65°C to 150C	P
High Temperature Storage	150°C	P
Latchup Sensitivity	1) QTP #002704 In accordance with JEDEC 17. Cypress Spec. 01-00081 (± 300mA)	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[3]	Failure Rate[4]
High Temperature Operating Life Early Failure Rate	4,357	0	N/A	N/A	0 PPM
High Temperature Operating Life[2,3] Long Term Failure Rate	1,920,312 DHRs	1	0.7	170	6 FIT

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate.
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

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[4] **EFR and LFR Rate based on GVT Technology and GVT Product Qualification an**

Reliability Test Data

QTP #: 002704

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HI-ACCEL SATURATION TEST (130C, 85%RH, 3.63V)PRE COND 192 HR 30C/60%RH							
CY7C1024AV33-BGC (7C1024V)	9024700	*340000217*	TAIWN-G	128	46	0	
STRESS: PRESSURE COOKER TEST (121C, 100%RH), PRE COND 192HRS 30C/60%RH							
CY7C1024AV33-BGC (7C1024V)	9038136	*610043675*	TAIWN-G	168	48	0	
STRESS: ESD-CHARGE DEVICE MODEL (500V)							
CY7C1024AV33-BGC (7C1024V)	9024700	*340000217*	TAIWN-G	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015 (2,000V)							
CY7C1024AV33-BGC (7C1024V)	9038136	*610043675*	TAIWN-G	COMP	9	0	
STRESS: STATIC LATCH-UP TESTING (125C, 6.95V, +/300mA)							
CY7C1024AV33-BGC (7C1024V)	9024700	*340000217*	TAIWN-G	COMP	9	0	
STRESS: TC CONDITION C, -65C TO 150C, PRE COND. 192 HRS 30C/60% RH (MSL3)							
CY7C1024AV33-BGC (7C1024V)	9024700	*340000217*	TAIWN-G	300	48	0	
CY7C1024AV33-BGC (7C1024V)	9024700	*340000217*	TAIWN-G	500	48	0	
CY7C1024AV33-BGC (7C1024V)	9024700	*340000217*	TAIWN-G	1000	48	0	

GVT73128A24 Product Qualification

Precondition - JESD - A113 - B

WT .35um GVT73128A24 Qualification			Condition Level 3, 192 hrs @ 30C / 60%RH			
Device	Lot Number	Package	In	Out	Rej.	Yield
GVT73128A24	W60098CA	100TQFP	80	80	0	100.00%

HTOL - MIL - STD - 883, Method 3015

WT .35um GVT73128A24 Qualification			Condition: Dynamic BI @ 150C, Vcc=3.6V, Vih=3 Reliability						
Device	Lot Number	Package	Read (hr)	0	24	184	500	TDH	FIT
GVT73128A24	W60098CA	100TQFP	SS/Rej	77/0	77/0	77/0	77/0	38,500	91.83

ESD - MIL - SRD - 883, Method 3015

WT .35um GVT73128A24 Qualification			Condition: Human Body Model		
Device	Lot Number	Package	Stress		2kV
GVT73128A24	W60098CA	100TQFP	SS/Rej		2,000V

FIT Rate Calculation

Pre . Cond	Fails	Deg. free	% conf.	1-cf	Chi sq	Activation energy	Derate temp	Accel factor factor	B/I temp Deg C	Total Device hrs	Best est. %fails per 500hrs	FIT
Y	0	2	0.6	0.4	0.92	0.7	55	259.17	150	38,500	0.90%	91.83

IC Latch-up - JESD78

WT .35um GVT73128A24 Qualification			Stress Condition				Vcc	
Device	Lot Number	Package	Read	Condition	Results	Forcing	Pos	Neg
GVT73128A24	W60098CA	100TQFP	SS/Rej	Class II	6	Voltage	5.4V	1.8V
				(125C)	0	Current	124mA	100mA

Technology Qualification Data

HTOL **Reliability Monitor**					
Dynamic BI @ 150C, Vcc=3.63V					
Read hr	0	24	184	368	500
SS	1960	-	1960	1959	725
Rej	0	0	0	0	1
SS	1885	1885	1885	1885	1885
Rej	0	0	0	0	0

HTOL **Qualification**					
Read hr	0	24	184	368	500
SS	435	435	435	-	435
Rej	0	0	0	-	0

WAFER LEVEL

Electromigration (EM)

Pattern	Fail Criteria >20% Change	Jmax>Jtsmc @ 0.1% CUM failure, 100k hoursn @ 110C, sample size 30 units. (Units in mA/um)					
		C92050		C92051		C92054	
M1 (0.4um)	1.0mA/um	>1.9	Pass	>3.74	Pass	>3.71	Pass
M1 (7um)	1.0mA/um	2.36	Pass	>1.59	Pass	>1.48	Pass
M2 (0.45um)	1.2mA/um	>5.61	Pass	>5.56	Pass	>5.46	Pass
M2 (7um)	1.2mA/um	2.32	Pass	2.16	Pass	2.07	Pass
Via (0.4 x 0.4)	0.34mA/um	>0.94	Pass	>0.94	Pass	>0.93	Pass
Via (0.45 x .45)	0.3mA/um	>1.04	Pass	>1.06	Pass	>1.05	Pass
Co (0.4 x 0.4)	0.41mA/um	>0.64	Pass	>0.64	Pass	>0.63	Pass

*Stress Conditions: 175°C

Hot Carrier (HEI)

Lot #	Gate	Fail Criteria= .1% CUM @ Vcc+10%> 0.2yr	Reading (year)	Results*
C92050	20/0.3um	Idsat Shift >10%	0.52	Pass
C92051	20/0.3um	Idsat Shift >10%	0.46	Pass
C92054	20/0.3um	Idsat Shift >10%	0.68	Pass

Test Condition: 10 pieces, Vds=4.5V for 12k minutes @ 25C.

Gate Oxide Integrity (GOI)

Pattern		C92050	C92051	C92054
(A) N-Well: 180,00um^2; Tox=70Å	Mode A Fail (%)	0	0	0
	Mode B Fail (%)	0.34	0	0
	Yield	99.66	100	100
(B) P-Well: 180,00um^2; Tox=70Å	Mode A Fail (%)	0	0	0
	Mode B Fail (%)	0.34	0	0
	Yield	99.66	100	100

Mode A: Vbd <=3.3V
Mode B: 3.3VVbd <8V